

Extraction of Barrier Heights in Si/Si_{1-x}Ge_x Heterojunctions with MIS Gates

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The advent of techniques to grow relatively defect-free, epitaxial films of Si/Ge alloys [1] led to the postulation of Si-Ge heterojunctions buried beneath MIS gates [2] to achieve high-performance MISFET's and minimize hot-carrier degradation. The poor quality of oxides grown on these alloys led further to the postulation of nitride growth on Si/Ge alloys, and a complementary device structure [3] to overcome the Type II band line-ups of Si/Ge heterojunctions [4]. Recent interest [5] in the Si/Ge MIS system shows the need for tools to extract the electrical barrier height of the Si/Ge heterojunction beneath the MIS gate.

This paper demonstrates a simple extraction technique based on low-frequency C-V measurements. The technique is considerably simpler than that applied in AlGaAs/GaAs heterojunctions using a Schottky gate [6]. It is evaluated using a one-dimensional, numerical simulator [7], modified to include Si/Ge alloy effects. The band-bending reference is changed to the vacuum level using the electron affinity rule [8]. Low-temperature and low-frequency capacitance details are also enhanced [9].

Figure 1 shows a buried HJ MISFET cross-section. Figures 2 and 3 show the 1-D energy bands for the MIS structure in two conditions: V_{TS} (buried layer inversion) and V_{TS} (surface layer inversion). Figure 4 shows the qualitative inversion charge versus gate voltage curve expected from a structure with two such threshold voltages. Using the band line-ups in Figures 2 and 3, it may be shown that:

$$\Delta E_V = \frac{q \int_{V_T}^{V_G} C_{LF} dV_G}{C_T}$$

This simple formulation assumes: no oxide or interfacial charge exists; the gate electrode is the same semiconductor as the surface semiconductor; no band-gap narrowing occurs in the gate electrode; the substrate depletion charge is ignored relative to the inversion charge; the surface semiconductor is relatively lightly doped (so that band-bending is linear, and not parabolic). Note that an undoped surface layer would maximize mobility in the MISFET. Since inversion charge is the integral of low-frequency capacitance from threshold to V_G in excess of threshold, the practical form for ΔE_V extraction becomes

$$\Delta E_V = \frac{\int_{V_T}^{V_G} C_{LF} \text{INV}(V_G) dV_G}{C_T(V_T)}$$

The denominator is another expression for C_T. Thus, one measures C_{LF}(V_G), integrates the inversion portion of C_{LF} to find inversion charge and V_{TS}, and the valence band discontinuity becomes known.

To test this simple method, low-frequency C-V curves were generated using the modified 1-D numerical simulator mentioned earlier. Figure 5 shows low-frequency, simulated C-V curves for T = 300K and 100K. Figure 6 shows a comparison between the barrier heights input into similar simulations, and the barrier heights extracted from the simple method of the first extraction equation. The structure simulated has T_{OX} = 300 Å, and a 100 Å surface silicon layer. As expected from the assumptions employed, better agreement is achieved for lower doping, and for low-temperature C-V curves, where KT/q is small compared to the barrier height.

In summary, a simple barrier height extraction method based on low-frequency capacitance is proposed for MIS structures with a buried heterojunction layer. The method is evaluated against a modified 1-D numerical simulator. Good agreement is achieved, especially for low substrate doping and low temperature. The method has been evaluated using the Si/Si_xGe_{1-x} system, but may be extended to any MIS system with a buried heterojunction layer.

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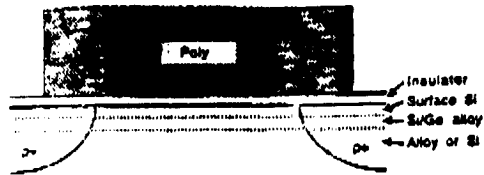


Figure 1. Cross-section of MISFET structure with buried heterojunction. Gate electrode is p⁺ poly. Substrate doping is 10¹³ cm⁻³, n-type. Extraction technique and simulations here relate to the MIS portion of this FET structure.

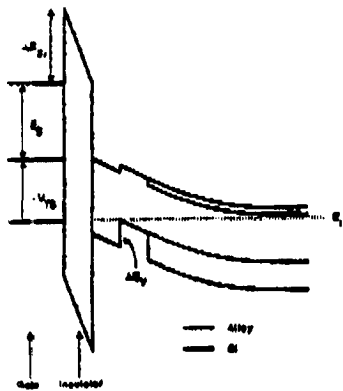


Figure 2. Band diagram for the device shown in Figure 1, in inversion, at threshold for the buried layer. The 2DHG is confined by the valence band discontinuity, ΔE_v . The substrate is $\text{Si}_{1-x}\text{Ge}_x$, where x may be less than unity. ΔE_g is the gate semiconductor-to-insulator band discontinuity. E_g is the band-gap of the gate electrode semiconductor. V_{TS} is the threshold voltage to invert the buried layer. ΔE_v is the quantity to be extracted.

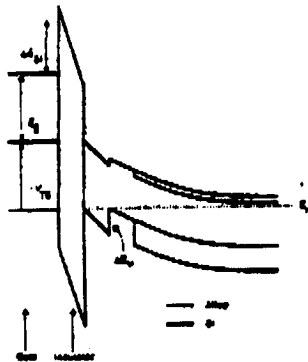


Figure 3. Similar to Figure 2, this band diagram is for $V_G = V_{TS}$, the threshold voltage to invert the surface semiconductor layer.

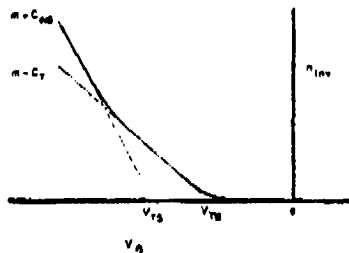


Figure 4. Schematic of inversion charge density n_{INV} vs. gate potential V_G , calculated from the low-frequency capacitance curve. m = slope of the charge vs. V_G curve. C_T is the total capacitance of the insulator and surface silicon layer. C_{INS} is the insulator capacitance alone.

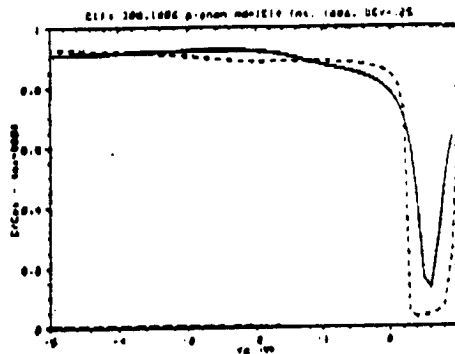


Figure 5. Capacitance curves for $N_d = 10^{14}$ cm⁻³. Solid line is for $T = 300\text{K}$; broken line for $T = 100\text{K}$. "DEV" is the valence band discontinuity ΔE_v .

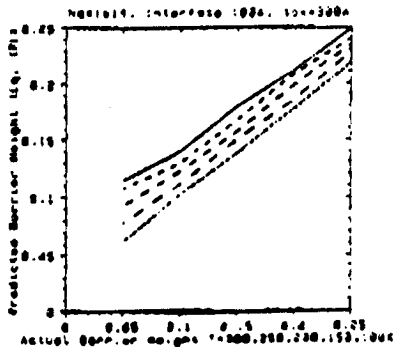


Figure 6. Extracted vs. simulation barrier heights using ΔE_v equation in the text, for $N_d = 10^{14}$ cm⁻³. Solid line is $T = 300\text{K}$; other curves decrease in temperature by 50K, so that the last curve is for 100K.