Thermal Considerations for Monolithic Integration of Three-Dimensional Integrated Circuits

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A major consideration for practical integration of 3D integrated circuits is compatibility of the thermal processes used to build new transistors in the vertical dimension, with sustained viability of the devices already fabricated beneath. Major contributions to the thermal profile of IC processes are laser-based anneals, rapid-thermal anneals and deposition processes, and traditional furnace processes for both annealing and film deposition. In this work, we consider the thermal compatibility of laser annealing of newly built 3D structures, with the ICs lying beneath.

INTRODUCTION

Integrated circuit scaling is entering the production phase of the 14nm node. Performance improvements will continue to accrue to the 10nm node, and probably to the 7nm node. It is unclear whether cost improvements at these next two nodes will also accrue. It is equally unclear whether nodes beyond 7nm will be practically attainable using foreseeable process technologies.

In this light, 3D integration of device and circuit structures becomes more attractive: provided, however, that the thermal profile of manufacturing new devices and structures in the vertical direction is compatible with the ongoing viability of the already-fabricated structures beneath [1-4].

Table I lists some of the major thermal steps in modern IC processing. These steps must be either replicated or replaced to fabricate 3D structure atop existing planar ones. This work looks at the use of laser annealing to replicate or replace critical procesing steps. Issues addressed are power absorbed as a function of laser wavelength, melt vs. sub-melt annealing, and peak temperature experienced by underlying structures.

MONOLITHIC 3D INTEGRATION

We term the main feature of our approach, “monolithic 3D integration.’ Fig. 1 shows our approach. Conventional devices are fabricated on a wafer in the traditional manner. After the addition of shielding layers and a final CMP step, a donor wafer transfers a fresh c-Si layer to the wafer. The fresh c-Si is separated from the donor wafer using cleaving along an H+ implant interface.

THERMAL CONSIDERATIONS

There are two types of thermal considerations in ICs: **operation**, and **processing**. We discuss only processing considerations here as they relate to 3D IC fabrication. (Some of our solutions also improve the thermal environment during operation.)

As seen in Table I, a number of thermal process steps are amenable to replacement with laser spike annealing (LSA). Table II shows the different approaches to LSA by three main manufacturers. Whether a whole-die approach, or a raster approach, is used, will depend upon the thermal conductivity and specific heat capacity of the underlying structures. For fast-transient, LSA processes, in our monolithic 3D approach the shield layer(s) have enough heat capacity to prevent temperatures in the underlying structures (esp. the copper metal lines, and the dopants in the transistor layers) from rising above 200 C.

Fig. 2 compares the fraction of energy absorbed for the three cases in Table II. In this calculation, normal incidence is assumed; the Ultratech approach does not use normal incidence, so that unabsorbed energy is primarily reflected, and not transmitted to underlying layers (an important consideration in overall annealing design).

Fig. 3 compares the energy absorbed in the transferred, surface Si layer, for conditions of melt and sub-melt annealing.

Fig. 4 shows the structural setup for a lumped-element transient simulation of an expected stackup involving a transferred Si layer atop a completed substrate. Fig. 5 shows the results of the transient simulation of this structure, for the (worst) case of melt annealing of the surface Si layer. The surface Si layer re-crystallizes within 2 ns. Neither the top nor bottom shield temperature exceeds 200 C; the underlying structures experience even smaller temperature excursions. No external thermal shunts are used: only the heat capacity of the shield layers is required.

REFERENCES

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Step	*Purpose*	*Time/Temp*	*Replace?*	*Laser?*
Si3N4 LPCVD	STI and well	30 min/700 C	Yes	No
Liner ox	STI	10 min/800 C	Yes	No
TEOS/densification	STI	20 min/1000 C	Yes	Yes
Implant activation	Well	20 sec/1000 C	Yes	Yes
Dummy ox	Gate	2 min/800 C	Yes	No
Dummy a-Si dep	Gate	20 min/600 C	Yes	No
Selective epi dep	SiGe and SiC S/D	20 min/700 C	Yes	No
Silicide formation	S/D contact	5 min/400 C	Yes	Yes
Implant activation	S/D, halo, VT	5 sec/950 C + LSA	No	Yes
BIL oxide + N	Gate	5 min/825 C	Yes	No
HfO2 post-ALD	Gate	30 sec/700 C	Yes	Yes

Table I: Major IC Thermal Processing Steps (Gate-Last FinFET)

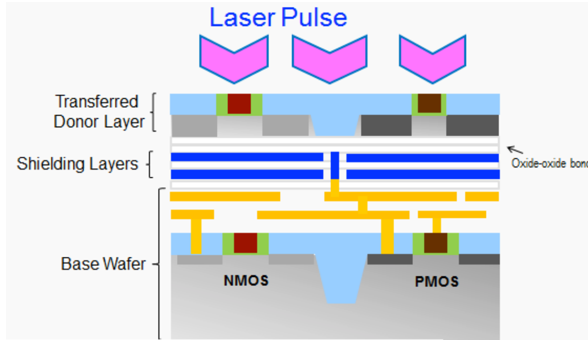

Figure 1: Monolithic 3D Integration.

Mfr	*Wavelength*	*Max Power*	*Duration*	*Approach*
Excico	308 nm	10 MW/cm2	10 ns	Whole-die
AMAT	808 nm	unknown	< 1 msec	Line/raster
Ultratech	850 nm + 10.6 um	unknown	< 1 msec	Line/raster

Table II: Laser Annealing Approaches.

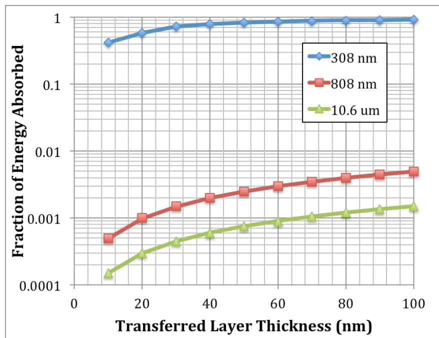

Figure 2: Comparison of LSA Approaches.

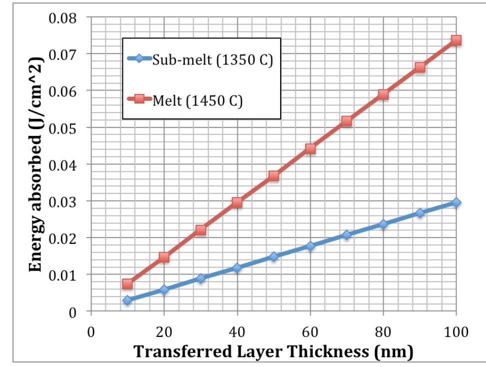

Figure 3: Energy Absorbed in Surface Si Layer.

Structure to Model	Layer Name	Thickness	Units
	Protect	0.005	um
	Transferred Layer	0.02	um
	Donor Bond Ox	0.05	um
	Acceptor Bond Ox	0.05	um
	Top Shield	0.25	um
	Inter-Shield	0.15	um
	Bottom Shield	0.25	um
	Inter-Shield	0.1	um
	IC8	0.1	um
	Ins8	0.09	um
	IC7	0.1	um
	Ins7	0.09	um
	IC6	0.1	um
	Ins6	0.09	um
	IC5	0.1	um
	Ins5	0.09	um
	IC4	0.1	um
	Ins4	0.09	um
	IC3	0.1	um
	Ins3	0.09	um
	IC2	0.1	um
	Ins2	0.09	um
	IC1	0.1	um
	Ins1	0.09	um
	IC0	0.05	um
	Ins0	0.05	um
	Substrate Si	775	um

Figure 4: Structure Setup for Transient Simulation.

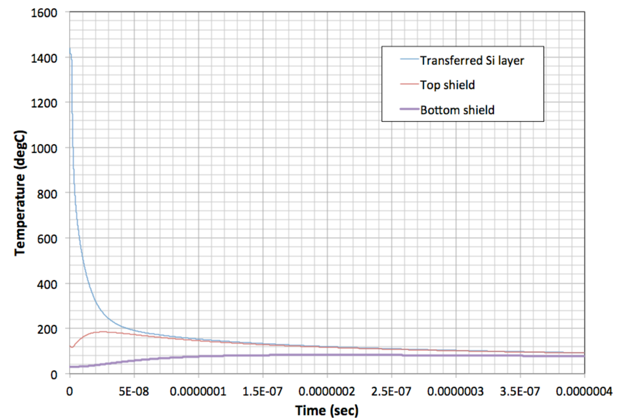

Figure 5: Transient Response of Monolithic 3D Stack for Melt LSA.