NMOS FET GATE CURRENT EFFECTS FOR REALISTIC BIASES AT 80K AND 300K

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ABSTRACT

This paper presents the first measurements of gate current at realistic drain voltages over the practical range of gate voltage operation. The data show the expected increase or decrease of gate current, as the temperature or bias changes. However, the observation of gate current in the drain avalanche regime for biases less than the barrier height shows these impact-ionized carriers must acquire an energy distribution beyond the band minimum as they approach the interface. It is further shown that an Auger mechanism cannot explain the observed gate current. Finally, the occurance of interface changes during the measurement is demonstrated, indicating the floating gate technique can be a sensitive monitor of these changes.

INTRODUCTION

Gate current measurements and analysis continue to frequent Si MOS literature (1-3), due to the relation of gate current to device reliability and the absence to date of a comprehensive simulator including gate current. This paper presents the first measurements of gate current at realistic drain voltages over the practical range of gate voltage operation. The data obtained demonstrate the expected increase or decrease of gate current, as a function of temperature and interface barrier height. Further, the observation of gate current in the drain-avalanche regime for biases less than the barrier height shows these impact-ionized carriers must acquire an energy distribution beyond the band minimum as they approach the interface. We show an Auger mechanism (4) cannot explain the observed gate current. Finally, we show that interface changes can be monitored by the floating gate measurement technique.

EXPERIMENTAL DETAILS

Fabrication details and substrate current characterization for these devices have been reported elsewhere (5). The measurement of gate current follows the techniques first used in (6) and later in (2). The measurement is an indirect one, relying on measurement of I_D vs. V_G and monitor of I_D vs. time for the floating-gate technique of (6) (see inset of Figure 1.) Thus, the gate current may be expressed as:

$$I_G = C_G(V_G)\,\frac{dV_G}{dI_D}\,\frac{dI_D}{dt}$$

A negative slope for dI/dt in an N-channel device becomes analogous to net electron injection into the gate electrode, thus decreasing the gate potential and reducing I_D. A positive slope corresponds to hole injection.

The measurements were carried out at a controlled temperature using an MMR Technologies refrigerator. The refrigerator lay inside a vacuum-enclosed four-probe station, which allowed easy implementation of the floating gate technique. An HP4145 controlled by an HP9836 was used to collect the data.

CHARACTERIZATION

A typical measurement of I_D vs. time is shown in Figure 1. After assuring the stability of I_D for a particular V_D and V_G bias, the gate probe is lifted at t=0; the channel current then becomes a sensitive measure of the charge on the gate as well as any interface charge changes, which are deduced from the change in I_D with respect to time. For the calculation of I_G, we use only the slope for t=0, since this slope represents a local oxide unstressed by the passage of gate charge. For the curves shown, I_D at t=0 was 5.855mA and 9.229mA for devices A and B, respectively.

Figures 2 and 3 show the I_G vs. V_G curves using two N-channel devices. Device A has dimensions of W/L=25/.7 in μm; device B has L_e=.75 μm. The low-field threshold voltages at 300K were .15 and .17V, respectively; at 80K, .39 and .41V. The gate capacitance was 0.7pF; t_{ox}=385Å. Drain voltages of 2.5V and 4.5V were applied, at temperatures of 80K and 300K. I_B vs. V_G was measured for each drain bias, before carrying out the I_G measurements. Each I_G calculation required between 50 and 1600 seconds of I_D monitoring, which effectively placed the device under DC stress. For most measurements, 100 seconds was sufficient. Between each bias point used for the I_G calculations, low-field transconductance (V_D =50mV) was measured in the forward and reverse mode to monitor interface charges, which might influence threshold voltage or surface mobility, in a sensitive fashion. Background leakage with the floating gate technique was measured to be less than 5×10^{-18}A.

DISCUSSION

Figure 1 shows the relative discharge of the gate capacitance due to hot electron emission, between 80K and 300K. The values of I_G for the two curves are 1.1×10^{-16}A for 80K, and 8.7×10^{-17}A for 300K; the substrate current values I_B are 440pA and 150pA at 80K and 300K, respectively. The 300K curve shows a greater departure from linearity than the 80K curve, for biases roughly in the same portion of the I_G characteristic. This sub-linearity means I_G is changing faster than expected based on thermionic emission considerations alone. A faster change is due to changes in the Si-SiO_2 interface at the point of gate current injection in the channel. Such changes consist of either interface state generation (and its subsequent ionization); or, increase in interface trapped charge due the gate current flux. From the predominantly linear characteristic at 80K, we infer these interface changes are temperature dependent, and occur more weakly at low temperature. Since I_D is constant for t<0 on the scale shown, heating or surface mobility changes are not responsible for the observed sub-linearity in I_D vs. t; the sub-linearity is also inconsistent with leakage currents from either of the biased device terminals.

The gate current curves in Figure 2 match expectations from previous work at higher drain biases (1-3). With V_D =4.5V, the highest potential in the device is greater than both the conduction and valence band barriers to thermionic emission at the Si-SiO_2 interface. In particular, we see the expected net hole current at low V_G , the so-called drain avalanche hot carrier (DAHC) net electron peak at mid-V_G , and the channel hot electron (CHE) peak at highest V_G . The offset in V_G of the two temperature curves is due to the threshold shift in the device between 300K and 80K, as well as some drain induced barrier lowering noted at V_D =4.5V and 300K. The steeper subthreshold slope at 80K accounts for the negligible hole current observed at that temperature.

Figure 3 shows the similar curves for V_D =2.5V - less than both the band discontinuities at

the interface. These data make good qualitative sense in terms of the band barriers: the maximum electron current decreases from 300K to 80K - and the hole current is completely absent. We note the V_D =2.5V curve shows no maximum value in the V_G range measured - an unexpected result, since the gate fields are less than the threshold for Fowler-Nordheim or direct tunneling. This may be due to the slightly punched-through nature of this device with no applied back bias.

Previously (8), CHE gate current was observed for biases less than the interface barrier. This was not hard to explain, since the CHE gate current comes from channel charge, possessing an energy distribution beyond the band minimum, scattered into and over the barrier. The observation of hole current for V_D=2.5V in Figure 3 shows that the DAHC gate current carriers must develop an energy distribution as they approach the interface. Assuming they start their travel toward the interface with zero energy, just after impact ionization, they would be unable to surmount the barrier thermionically unless they developed such a distribution: the potential between the generation and injection points is less than the barrier height. This is true for the DAHC electron peak in Figure 2, as well. Any model of DAHC gate current, then, must include the development of such an energy distribution.

Figure 4 shows the result of plotting the gate current vs. the Auger product n^2p (or $I_D{}^2I_B$) for electron emission into the gate. From (4), one would expect a unity slope on a log-log plot from this mechanism - particular for V_D =2.5V, the low-field regime where this mechanism is supposed to be important. For our devices, at V_D =4.5V we do not observe such a linear relationship. Further, for V_D =2.5V, the slope has the wrong sign. We do not plot the hole current vs. its Auger product counterpart, since the results also show an absence of linearity or unity slope. Thus, we find no evidence for Auger-assisted emission in our devices.

Changes in the interface occur during the I_G measurement, as mentioned in the discussion of Figure 1. Figure 5 shows the I_G vs. V_G characteristic derived using the technique of (2) from the T=300K, V_D=4.5V, V_G=6.5V measurement. The initial exponential slope is due to capacitive charge redistribution currents associated with lifting the gate probe. The arrows indicate the I_G and V_G values at t=0, used in Figures 2 and 3. The remaining exponential characteritic is consistent with an increase of the interfacial barrier to thermionic emission, according to:

$$I_G \sim \exp(\frac{-q\Delta\phi_B}{kT_e})$$

where $\Delta\phi_B$ is the barrier height change, and T_e is the carrier temperature.

The interface change is shown further in Figure 6; the arrows indicate the order of measurements for the 300K curve in Figure 3. When the attempt was made to refine the DAHH characteristic, electron current was measured where hole current would have been expected, had the interface remained unchanged during the measurement. The effect is interpreted as follows. The DAHH measurements - 1600 seconds in duration, as opposed to the usual 100 seconds for electrons - raised the local barrier to hole transport. When V_G was raised to 1.0V from 0V, net electrons were measured because this $\Delta\phi_B$ to hole transport suppressed the hole emission below the electron emission. Thus, Figure 6 also shows both electron and hole emission must be considered in the DAHC regime.

CONCLUSIONS

We have presented measurements of NMOS FET gate current, at drain and gate biases typical of normal device operation, at 80K and 300K. The results are consistent with previous data at higher V_D, and with qualitative expectations from thermionic emission over the valence and conduction band barriers. We have shown the results are not well-described by an Auger mechanism. The observation of DAHC gate current at low biases means these carriers must develop an energy distribution as they approach the interface. The gate current measurements given thus provide a benchmark for developing gate current models in such simulators.

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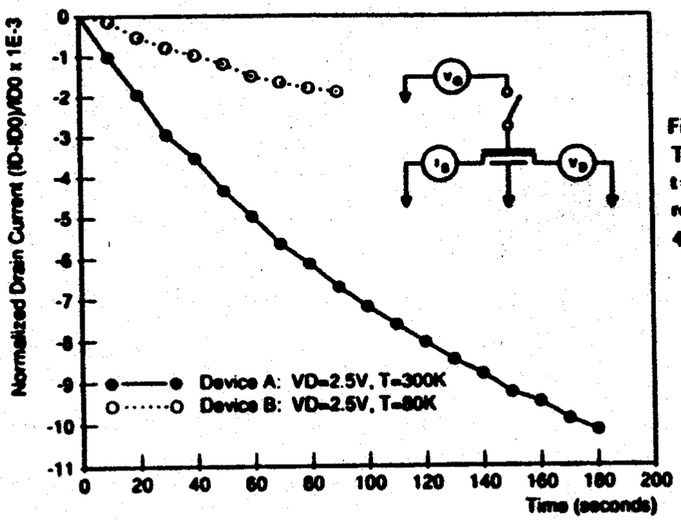


Figure 1. Floating gate measurement technique. The switch on the transistor gate is opened at t=0 (see Inset). Shown are ID vs. t curves for roughly the same IG; VG for the filled circles is 4.5V, and 5.0V for the open circles.

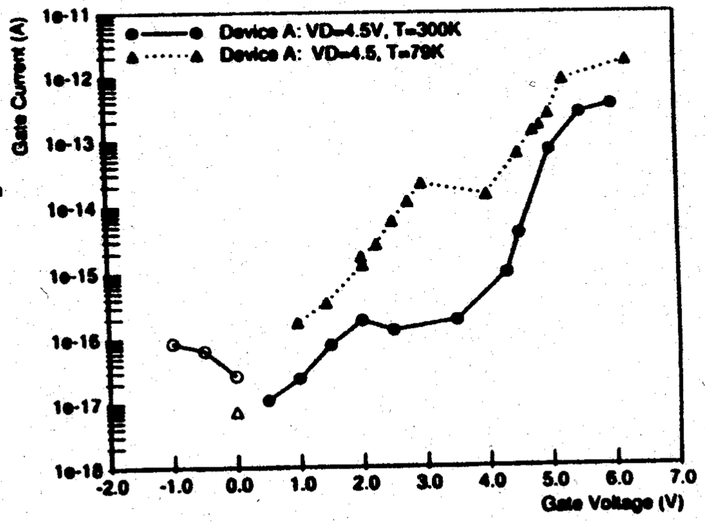


Figure 2. Gate current for VD=4.5V. Open symbols are hole current; closed symbols are electron current.

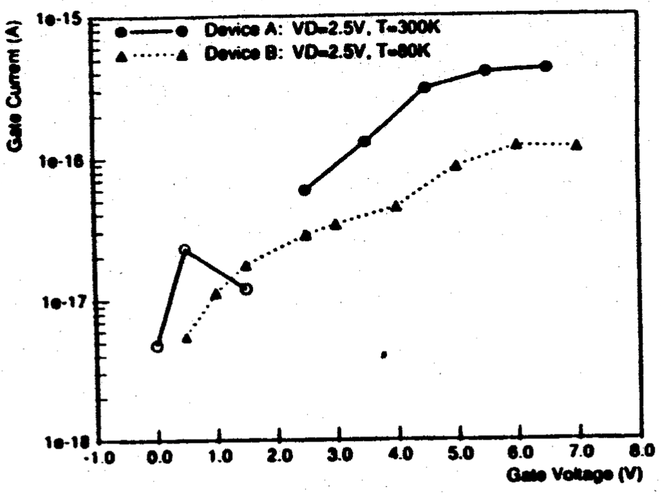


Figure 3. Gate current for VD=2.5V. Open symbols are hole current; closed symbols are electron current

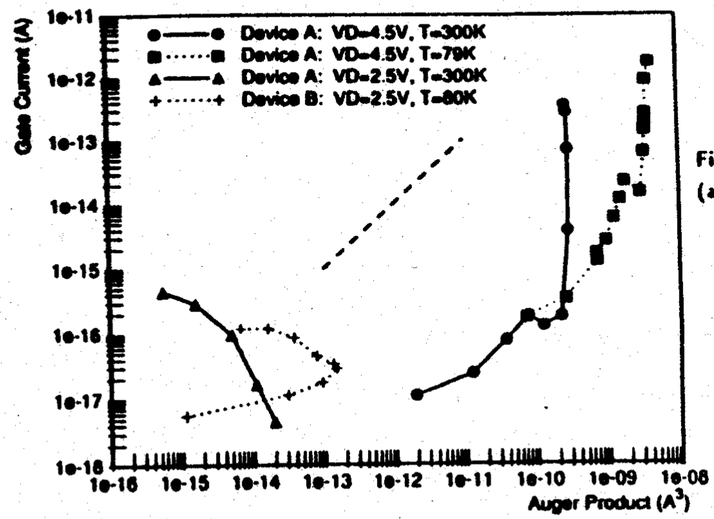
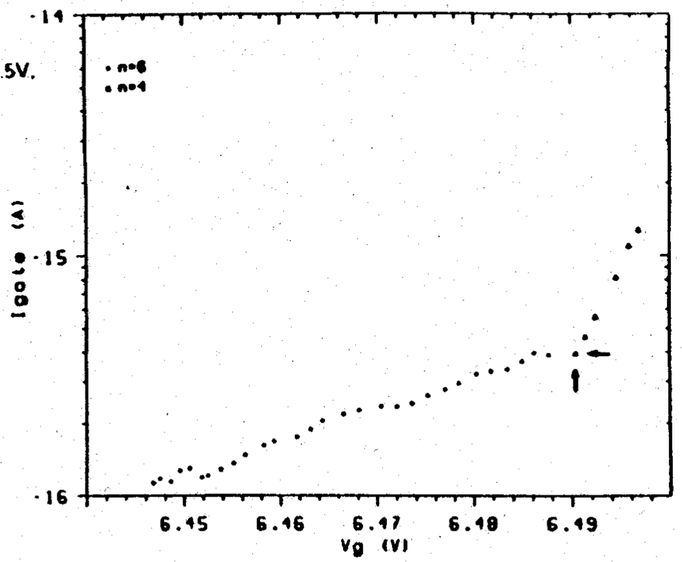


Figure 4. Gate current vs. Auger probability (after Ref.(4)). The Auger product is $I_D{}^2 I_B$

Figure 5. Gate current extraction for V_G=6.5V, V_D=4.5V and T=300K. The arrows indicate the I_G and V_G values at t=0.



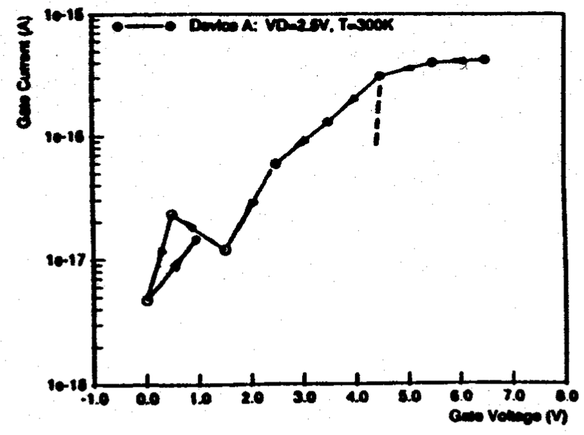


Figure 6. Interface changes and the dual nature of charge emission into the gate. Shown is the 300K curve of Figure 3. The arrows indicate order of measurement. See text for discussion.