(N_{int}) can be modeled as having two components. The first component is constant and has a value of $\sim 5\times10^{10}cm^{-2}$ which is consistent with Si/SiO_2 interface charge densities determined from V_t analysis of thicker gate oxide (300Å-600Å) MOSFETS. The second component is approximately proportional to t_{ox}^{-2}, and becomes significant only for t_{ox} less than 100Å. Thus, it appears that as the oxide thickness is decreased, the inversion layer electrons begin to "see" coulombic scattering centers at or near the SiO_2/Gate interface.

A detailed analysis of the mobility measurements and the numerical model will be presented.

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IIIB-4 Analysis on Selective Writing for Taper Isolated RAM Cell—S. Kurosawa, T. Ishijima, M. Takada, K. Terada and S. Suzuki, Microelectronics Research Laboratories, Nippon Electric Co., Ltd., 4-1-1, Miyazaki, Miyamae-ku, Kawasaki, 213, Japan, (044) 855-1111, Ext. 2117.

A selective writing mechanism for Taper Isolated (TI) RAM cell (1) was analyzed and its performance capabilities were evaluated by using a two dimensional process-device simulator and experimental test devices.

The TI RAM cell is one of the most prospective candidates for future VLSI memories, because of its small cell size and internal cell gain. The cell consists of a single buried n-channel MOSFET. Its channel resistance is changed with holes stored in a potential well at the shallow p-region underneath the gate electrode. However, hole injection mechanism, or selective writing mechanism, has not yet been understood, because the mechanism itself changes with the change in LOCOS isolation structure or channel stop boron impurity profile. Therefore, quantitative analysis is necessary for accurate cell design, and in consequence, for proper cell evaluation.

Two dimensional analysis across and along the channel reveals the following points:

1) Device structure at the channel edges determines the writing mechanism. If the channel stop boron significantly compensates for the n-type impurity at the channel edges, a parasitic pMOS LOCOS-taper-transistor action governs the writing operation. Otherwise, a vertical PNP bipolar-transistor action does.

2) For the cell using the parasitic pMOSFET, the inhibit "0" writing characteristic is poor, because the substrate impurity concentration for parasitic pMOSFET (n-region) is low and its substrate potential cannot be sufficiently controlled through the word line.

3) Selective "1" writing is realized only for a short channel cell, by modulating the potential under the p-region with source (word line) potential and controlling the hole injection from the substrate. However, the channel length has to be precisely controlled, because the inhibit characteristic as well as required operation voltage swing are very sensitive to the channel length.

To obtain the ideal cell using the bipolar-transistor action, the trench isolation technique (2) was used in test devices. Calculated and experimental characteristics are in good agreement. They showed that the required operation voltage swing increase per channel length decrease was 0.3V/0.2μm for about 2μm channel length cell. Using an accurate cell design, complete inhibit writing characteristics and high "1"/"0" current ratio (>6) were obtained for a 3μm/2μm channel width/length test cell in -3,0,3V operation.

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IIIB-5 Current Characterization of SCR Latch-Up in CMOS Circuits—J. Patrick Dishaw, Kim Kokkonen, Albert Matthews and Albert Henning, Intel Corporation, Santa Clara, CA 95051, (408) 496-9140.

We present a new characterization methodology for SCR latch-up in CMOS circuit using current induced latch-up. Previous work on SCR latch-up analyzed the latch-up performance of the technology using the static breakdown voltage of the SCR [1]. Though illustrative of some aspects, this

technique does not lend itself to design rule analysis since CMOS circuits operate at a fixed voltage. We have developed a characterization methodology which deals with this issue by analyzing latch-up using currents injected into the base regions of the coupled bipolar transistors of the SCR [2]. Such an analysis elucidates the role of circuit parasitics on latch-up [3]. This leads to design rules and optimum processing for CMOS circuits.

To confirm this methodology, data has been taken on SCR latch-up using a state of the art CMOS process. N epi on an N+ substrate was used with a p-well depth of 2.5 microns and junction depths of .25 microns. The current latch-up modes were separated into PNP (lateral bipolar in the SCR structure) and NPN (vertical bipolar) device induced latch-up. Latch-up currents for PNP induced latch-up followed a relative I(PNP) = Vbe(NPN)/Rwell with Vbe(NPN) = 0.64V. Latch-up currents for NPN induced latch-up followed a relation I(NPN) = Vbe(PNP)/Rsub with Vbe(PNP) = 0.68V. The reduction in Rsub obtained with the use of N type epitaxial silicon on an N+ substrate effectively eliminates this mode of latch-up. The effect of elevated temperature was also considered. The net effect was to decrease Vbe(PNP) and Vbe(NPN) in the above relations to 0.45 and 0.37V respectively at 125°C where the parasitic resistances Rwell and Rsub have also been evaluated at this temperature. Using this methodology we find that for a 4μ N+ to P+ space, latch-up can be controlled by placing p-well taps within 40μ of all N+ diffusions within the well, and by limiting the P+ to substrate forward bias to $\leqslant$0.2V d.c. or $\leqslant$0.6V pulsed for $\leqslant$10 ns.

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IIIB-6 "CODMOS" — A Depletion MOSFET Using Fixed Oxide Charge—R. Kazerounian and W.G. Oldham, Department of Electrical Engineering and Computer Sciences and the Electronics Research Laboratory, University of California, Berkeley, CA 94720, (415) 642-3221.

We present a new depletion mode n-channel device structure which functions over temperature range 77°-400°K. This charged oxide depletion MOS device uses Cesium ion implantation of silicon dioxide of the MOS structure. Cesium ions have shown great stability in SiO_2 under temperature bias stressing [1,2]. The presence of these positive ions in the gate oxide turns on a channel under zero gate voltage. Overcoming of donor freeze out problem observed in conventional depletion devices [3] and improved subthreshold and substrate sensitivity behaviors are expected using this structure.

A Standard local oxidation n-channel process has been used for fabrication at test devices. Low energy (40 keV, Rp = 190Å, ΔRp = 50Å) Cs^+ ions are implanted after growing 650Å gate oxide in 1000C dry O_2 with doses of 3.46e12 and 6.92e12 cm^{-2}. Conventional depletion devices are also fabricated by (120 keV, 1.488e12 and 2.8e12 cm^{-2}) arsenic implantation of SiO_2.

It is observed that the activation of cesium implanted ions depends on the post implantation annealing cycles. Cs^+ implanted devices have been fabricated with a room temperature threshold voltage of -6.4 volts which shifts to -3.2 volts at 77°K. This is compared with 99% positive shift for conventional depletion devices. It is suspected that freeze out of the interface states generated by Cs^+ ion implantation is the cause of threshold shifts in the CODMOS devices. Better substrate sensitivity of CODMOS devices is observed over conventional depletion devices.

Successful CODMOS device test results confirm the feasibility of this design technique in fabrication of high performance n-channel depletion mode devices especially when low temperature operation is desired.

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