Failure Analysis Using Scanning Kelvin Probe Microscopy

Session O-5

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Abstract

A novel combination of scanning Kelvin probe and atomic force microscope has been used to examine fabrication related defects in integrated circuit microstructures on a sub-micron scale. By measuring the potential difference which minimizes the electrostatic force between a probe and surface of a sample, we estimate the work function difference between the probe and surface. The work function difference is related to the electrical properties of the materials, and anomalies in the work function profiles may be attributed to defects near the surface of the sample under test. Our measurement system has a lateral resolution better than 100 nm and a sensitivity of 5 mV in a 1 Hz measurement bandwidth. All measurements are performed in ambient atmosphere with minimal sample preparation.

A brief overview of the measurement technique will be presented, along with several examples of failure analysis with our system. Measurements presented will include imaging of dislocations on silicon substrates, bird's beak induced stresses at the edges of poly-silicon gates, dopant anomalies in CMOS transistor gates, surface charge on oxide in a field of DRAMs, and electrical defects in the channel region of an n-channel MOSFET.

1 Introduction

As the critical dimensions of integrated circuits (IC) are reduced and the density of devices is increased it becomes more costly to be able to probe their electrical operation for Failure Analysis (FA). A probing pad for every component is impractical, and die size constraints or interconnect issues are limits to accessible areas of the chip. An optimal FA tool needs to meet the following criteria: inspect a die at any internal location, measure quantities on scales smaller than minimum feature sizes and switching times, be minimally invasive, require minimal sample preparation, yield high through-put, yield consistent measurements, and be cost effective.

There have been several novel techniques developed for use in FA including probing via electro-optics [1], electron beams [2], inductive [3] and capacitive [4, 5] near-field imaging, electro-acoustics [6], photoconduction sampling [7], and variants of the atomic force microscope (AFM) [8–17]. Each of these techniques addresses some of the criteria mentioned above.

We attempt to address the issue of FA with a modified heterodyne interferometer AFM [18] operated as a force-based scanning Kelvin probe microscope (SKPM) [11]. The SKPM is similar to the traditional displacement current or vibrating reed Kelvin probe [19, 20], using the electrostatic force instead of displacement current to determine the electrostatic potential difference (EPD) between a probe and the local surface of a sample. The EPD is directly related to the work function difference (WFD) between the probe and the sample since the finite probe size leads to

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the EPD being a weighted average of the local WFD [21]. Variations in the measured EPD may be attributed to changes in local material properties, and anomalous measurements result from defects in the materials. To date our emphasis has been on examining a qualitative relationship between the measurements and defects.

The remainder of this manuscript will be devoted to describing the behavior of the system and presenting some examples of its use in IC analysis. These measurements of FA include imaging of dislocations on silicon substrates, bird's beak induced stresses at the edges of poly-silicon gates, dopant anomalies in CMOS transistor gates, surface charge on oxide in a field of DRAMs, and electrical defects in the channel region of an n-channel MOSFET.

2 System

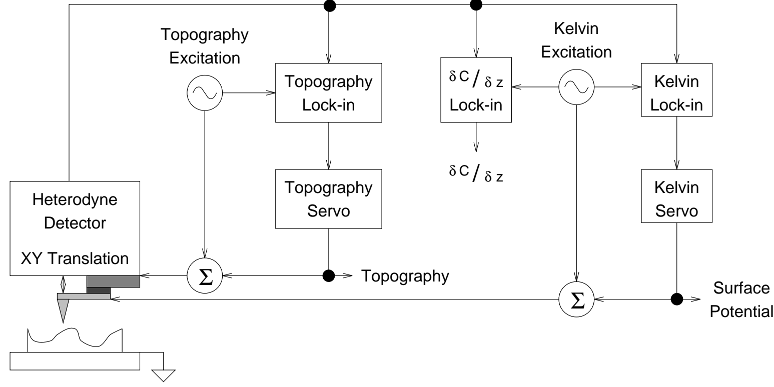

Figure 1: System level diagram of the IBM/Dartmouth College SKPM.

Our SKPM is a modified AFM that is on loan to Dartmouth College from IBM – Essex Junction. Figure 1 shows a schematic of the SKPM that we have built. A set of piezo stacks and mechanical levers (Piezo Flex stage [22]) is used to adjust the lateral position of either a silicon [23] or tungsten probe over a sample with a 100 μm range and 1 nm positionability. A heterodyne interferometer is used to detect the simultaneous deflections of the probe due to the atomic scale forces at several different frequencies.

The probe is oscillated mechanically with a piezoelectric bimorph at a frequency slightly higher than the dominant mechanical resonant frequency of the probe. Changes in the amplitude of oscillation at this frequency are used to adjust the spacing between the probe and sample to maintain a constant van der Waals (vdW) force gradient. This yields an approximation of the surface topography.

DC and *ac* potentials are applied between the sample and the probe for measurement of the EPD and spatial variations in total capacitance of the probe/sample system $\left(\frac{\partial C}{\partial z}\right)$. The *ac* component is at a frequency corresponding to another resonant peak in the probe's mechanical frequency response spectrum. The mixing nature of the electrostatic force causes deflections of the probe at the oscillating frequency and its harmonic [11]. The *DC* component is adjusted to minimize the amount of deflection detected at the fundamental frequency. The magnitude of the harmonic is monitored to obtain the capacitance measurements.

The feedback voltages needed to maintain a constant force gradient or minimize the electrostatic force and the magnitude of the capacitive signal are collected with a computer via an analog-to-digital converter board. We then use the collected data to generate 2D vdW/EPD/$\frac{\partial C}{\partial z}$ surfaces or grey-scale images of the measurements for further analysis and processing.

Since the vdW and electrostatic forces are both attractive in nature, there is only one unique solution point for the system when both control loops have stabilized. Thus, the raw image data may be used to obtain qualitative information about the sample under study without the need for extensive data analysis. However, obtaining quantitative information about the sample surface requires data deconvolution. Theoretical details of the forces and feedback upon which the system operation is based may be found in the literature [11, 18, 24–27].

This instrument has been used at Dartmouth College for the past year as an FA tool. The system consistently achieves lateral resolutions under 100 nm, a vdW noise level of 0.5 Å/$\sqrt{\text{Hz}}$ measured in a 100 Hz bandwidth, and an EPD noise level of 5 mV/$\sqrt{\text{Hz}}$ measured in a 160 Hz bandwidth. The system is capable of achieving lateral resolutions of 25 nm, a vdW noise level of 0.1 Å/$\sqrt{\text{Hz}}$, and an EPD noise level of 1 mV/$\sqrt{\text{Hz}}$.

All measurements have been performed in ambient atmosphere. Successful measurements have been taken on samples prepared under a variety of conditions, from cleaning the surface with compressed air to buffered HF dips. Measurement times are dependent upon the desired resolution and scan size. The majority of the scans shown in this manuscript took 15 to 20 minutes to generate. Measurements have been shown to be reproducible over a 2 month period of time. A probing pad is not required because of the non-contact nature of the measurement system, enabling the investigation of the electrical properties of RAM cells in the middle of arrays.

3 Measurements

3.1 Dislocations

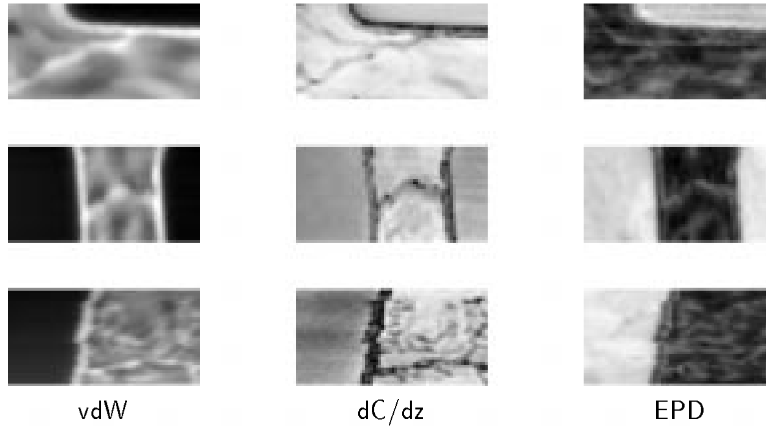

Figure 2: Scans of dislocations near field oxide regions in the substrate of a CMOS memory chip imaged with the SKPM. The $\frac{\partial C}{\partial z}$ measurements appear to be the most sensitive to the electrical effects of the dislocations.

The first FA sample provided us with many interesting defects. Figure 2 shows several dislocations that were imaged with the SKPM. The sample is a CMOS memory chip. All oxide and metal layers had been chemically removed from the sample, leaving behind the substrate and poly-silicon gates. The dark regions in the vdW images of Figure 2 correspond to regions where the field oxide (FOX) had been present. The top two rows are scans of $\approx 3\ \mu\text{m} \times 1\ \mu\text{m}$ and the bottom row is $\approx 5\ \mu\text{m} \times 3 \mu\text{m}$.

The dislocations may be seen in the vdW images, but they are not easily distinguished from the surrounding substrate. The $\frac{\partial C}{\partial z}$ images clearly show the dislocations. The top and bottom EPD images do not show the dislocations, while the middle EPD image does indicate the presence of the dislocation. Since the dislocations primarily appear in the $\frac{\partial C}{\partial z}$ and not the EPD images, this indicates that the dislocations have a small effect upon the WFD of the surrounding material but have a measurable effect upon the charge signal.

3.2 Bird's Beak Stress

Our first series of scans also imaged what appear to be residual effects of bird's beak stress on poly-silicon gates due to FOX encroachment. Figure 3 shows grey-scale images and line profiles from a different area of the same sample shown in Figure 2. The dark region in the vdW image is the region where FOX had been present and the bright horizontal stripe is a poly-silicon gate. The left scans are $\approx 3.0\ \mu\text{m} \times 3.0\ \mu\text{m}$ in size.

The vdW image indicates that the surface of the gate is flat. The section of the gate that had been in contact with FOX is etched from the sample preparation. The EPD signal shows higher contrast near the FOX edge of the gate, which drops off to a uniform value at 0.5 μm from the FOX. This change in contrast was seen in the EPD images at the FOX edge of every gate scanned on this sample. We attribute this to changes in the poly-silicon band-structure due to stress induced from the growth of a bird's beak in the gate oxide at the FOX interface. The capacitance signal shows mostly uniform contrast.

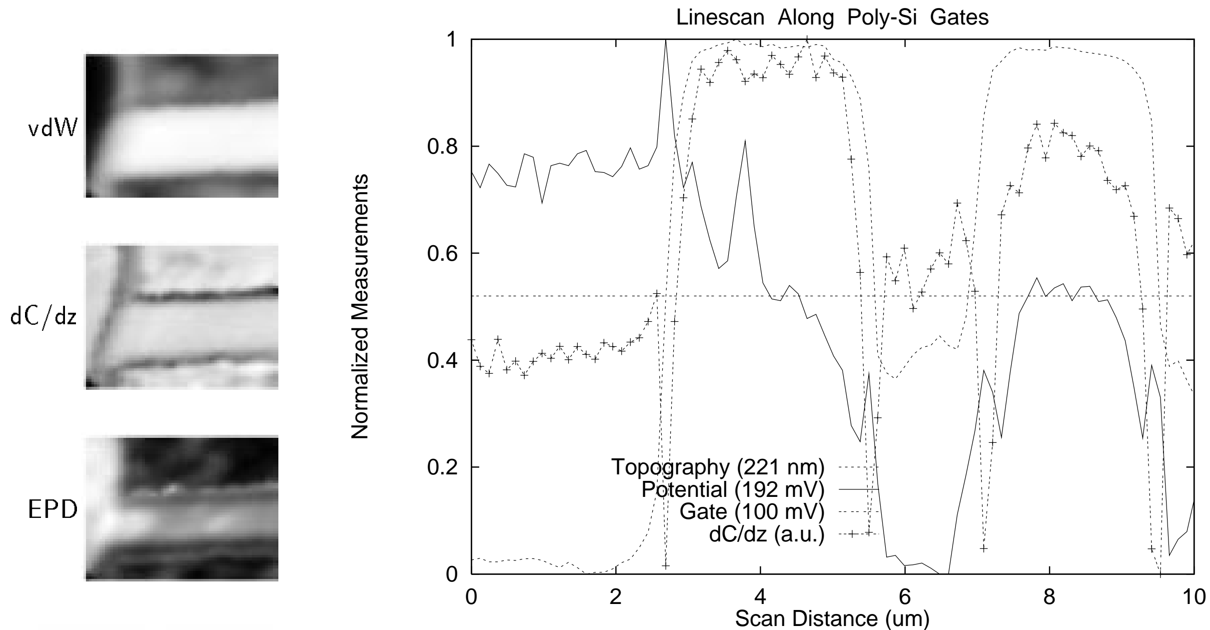

Figure 3: Grey-scale images and line profiles of measurements from poly-silicon gates showing residual effects of bird's beak stress. The EPD signal has an anomalous feature at the left edge of the gate due to the stress. The profile is taken diagonal to the direction of the scan and through two adjacent poly-silicon gates (second gate is not shown in the grey-scale images), and shows the magnitude of the effect upon the EPD signal of the gate. The values in parentheses are the full scale changes of the normalized signals. The vdW signal indicates an unusually thin poly-gate stack (see text).

The profile plot shows normalized values along a line through the measurements taken diagonal to the direction of the scan. The profile starts in the FOX region (0.0 to 2.5 μm) and intersects two poly-silicon gates (one at 2.5 to 5.0 μm and the other at 7.0 to 9.5 μm). The ridges in the EPD and the valleys in the $\frac{\partial C}{\partial z}$ signals on either side of the poly-silicon gates are due to the finite probe size and lateral electrical signals [5, 21].

The horizontal line indicates the mean EPD associated with the gates in regions that do not show the effects of the bird's beak stress. The effect of the bird's beak stress changes the EPD of the gate by 50%. The $\frac{\partial C}{\partial z}$ profile shows that the defect affecting the EPD signal does not affect the charge signal, indicating that the defect is near the surface of the poly-silicon gate and not in the oxide or channel. The reason for the difference in the $\frac{\partial C}{\partial z}$ signal between the two gates is discussed in the following section.

The vdW profile indicates that the poly-silicon gate stack is only 221 nm, which is quite low. This is the result of poor calibration for the vdW control loop. We have three calibration standards that are used to obtain as accurate a measurement of topography as possible with the vdW loop. However, the scaling factor is only accurate for a particular setting of the feedback loop. If the settings are changed, then the measurement needs to be recalibrated. The electrical measurements from this sample were of greater interest than any topography measurements, so we were not rigorous in our topography calibration.

3.3 Dopant Anomalies

The primary goal for FA on the sample described in the previous sections was to determine if dopants had been implanted through the poly-silicon gates and into the channel. If dopants were in the channel or the gate oxide was defective, the surface nature of the EPD signal would show very little difference between the functional and failing gates. On the other hand, the $\frac{\partial C}{\partial z}$ signal should show differences since it depends upon the total charge between the probe and electrical connections to the sample.

The left set of grey-scale images in Figure 4 shows the results of measurements on functioning and failing gates. The scans are ≈ 3.0 μm $\times$ 5.0 μm in size. The vdW signals indicate that there are no topographical defects along

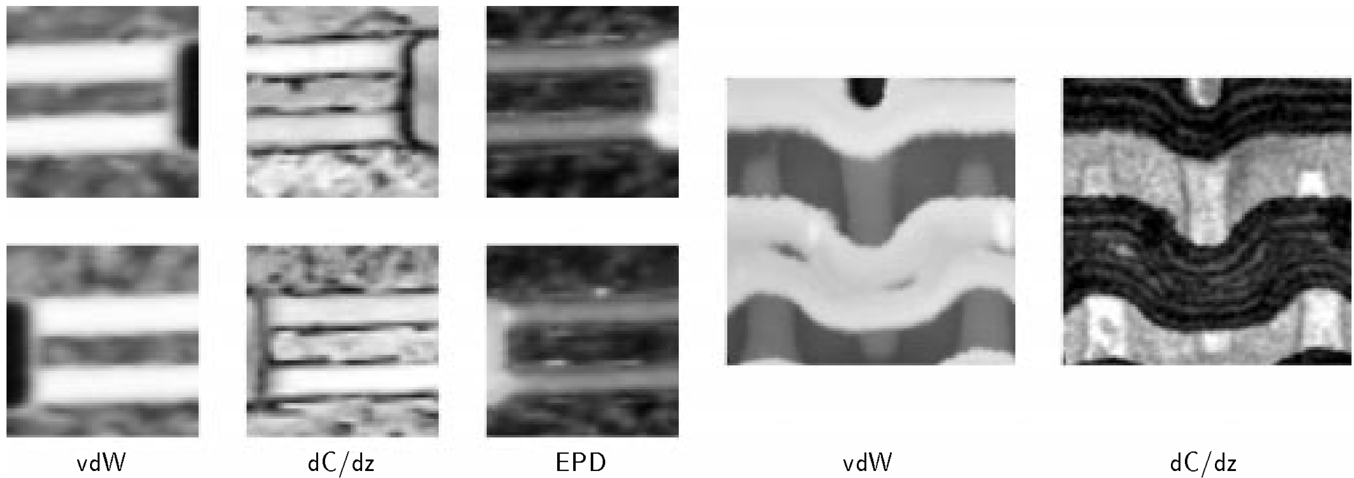

Figure 4: Scans of two different CMOS memory chips showing dopant anomalies in the channels of the gates. The left images are from different areas of the same sample from Figures 2 and 3. The right images are from the same area shown in Figure 5 without the presence of any surface charge.

the gates, and the EPD signals indicate small fluctuations (not visible in the figures shown) which are probably due to variations in dopant density or WFD due to grain orientation. And as in the previous section, the EPD signal appears to image bird's beak stresses for the gates.

However, the $\frac{\partial C}{\partial z}$ signals indicate that there is a difference between the two gates imaged in each scan (which can also be seen by examining the two gates in the line profile of Figure 3). For the top row of images, the upper gate was functional and the lower gate was failing. For the bottom row of images this was reversed, with the upper gate failing and the lower gate functional. In both cases the failing gate showed the same change in contrast, and was consistent with electrical and TEM measurements made on the gates at IBM – Essex Junction.

The right images in Figure 4 are from scans made on a different CMOS memory chip. The scan is $\approx 4.0\,\mu\text{m}\times 3.0\,\mu\text{m}$ in size. The sample was mechanically polished and only the metal layers were removed by selective etching. The light areas in the vdW image are oxide. Metallic word lines ran along the channels between the oxide regions. Three adjacent transistors are imaged. Two gates lie in the lower word line space, and one lies in the middle of the upper word line. Only the vdW and $\frac{\partial C}{\partial z}$ images are displayed since the large surface relief kept the EPD signal from detecting significant contrast. The EPD image in the upper left set of scans from Figure 5 is an indication of the lack of signal contrast from these measurements.

The failing transistor in this case is the one on the left of the image. The problem is attributed to the presence of a poly-silicon grain at the end of the leftmost transistor within the space where the upper word line ran. The $\frac{\partial C}{\partial z}$ signal also indicates that the gate region of the left transistor is electrically different than the gates of the other two transistors. Two darker regions may be seen in the gate of the left transistor in the $\frac{\partial C}{\partial z}$ image, whereas the gates of the other two transistors do not show significant contrast variations.

3.4 Surface Charge

During the scans of the DRAM memory chip shown in Figure 4 and discussed in the previous section, the tip contacted the surface of the oxide momentarily. The result was a deposition of a small quantity of charge on the oxide, which the SKPM was able to detect with all three measurement modes. Figure 5 shows scans made with and without the presence of the surface charge on the oxide. The left scans are $\approx 7.0\ \mu\text{m} \times 4.0\ \mu\text{m}$, and the right scans are $\approx 2.0\ \mu\text{m} \times 2.0\ \mu\text{m}$.

The deposited charge may be seen a third of the way from the bottom and near the middle of the images in the lower row of Figure 5. The charge was deposited on the oxide over the failing transistor described in the previous section. As can be seen in the $\frac{\partial C}{\partial z}$ image with the charge present, the anomaly in the $\frac{\partial C}{\partial z}$ signal for the gate described in the previous section becomes more visible in the presence of the charge (immediately to the left of where the charge is imaged in the $\frac{\partial C}{\partial z}$ measurements).

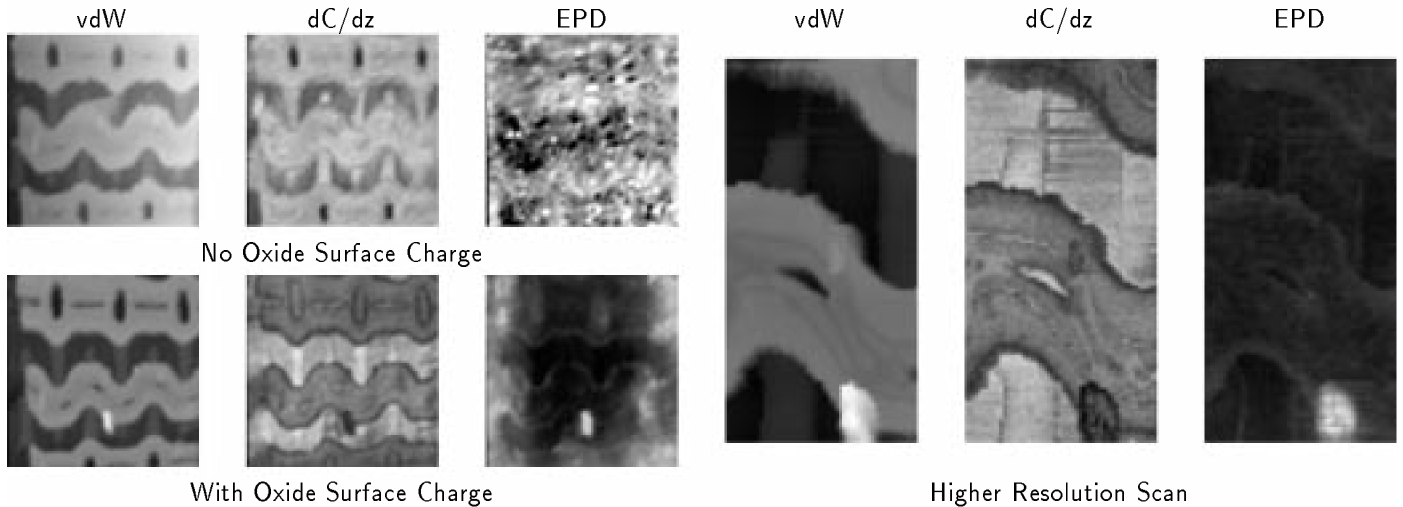

Figure 5: Scans of DRAM memory cells in which surface charge was deposited on oxide. The sample is the same as shown in the right images of Figure 4. The change in contrast for the $\frac{\partial C}{\partial z}$ signal is due to the operation of the SKPM (see text). The lack of contrast for the top left EPD image is from the large surface relief on the sample. The images show how the presence of the surface charge has an impact upon the EPD signal over a large surface area and minimally affects the vdW and $\frac{\partial C}{\partial z}$ signals.

In terms of the lateral extent of the surface charge, the vdW and $\frac{\partial C}{\partial z}$ signals are minimally affected. The EPD signal is significantly affected by the presence of the surface charge. The trapped charge leads to curvature of the energy bands in the space about the charge, which changes the WFD and hence the measured EPD. It is unusual that the effect is not symmetrical about the charge point, but instead about the area of the failing transistor. The nature of this observation hasn't been determined at this time.

Using simple models for the probe and sample system, we have determined that the feature represents 6 units of electrical charge. This is easily within the resolution shown by other researchers [9, 28], but recent analysis of the SKPM measurements indicates that this value needs to be recomputed [21]. The correction will likely be less than an order of magnitude. The computations also assumed that the charge was uniformly distributed, but the higher resolution scan indicates that the charge is present at two separate spots of the oxide.

The change in contrast of the $\frac{\partial C}{\partial z}$ signal with and without the presence of the surface charge is related to the behavior of the SKPM and not to the sample. We do not servo the $\frac{\partial C}{\partial z}$ signal – a lock-in amplifier is used to detect, rectify and filter the data. Variations in the phase of the lock-in amplifier to the applied electrical signal can lead to changes in the $\frac{\partial C}{\partial z}$ contrast, as seen in this set of images.

3.5 N-Channel MOSFET

One of the more promising features of the SKPM is the ability to measure dopant profiles in IC devices [29]. Figure 6 shows grey-scale images of the vdW and EPD signals from a 5 μm $\times$ 5 μm scan of two adjacent n-channel MOSFETs. The primary goal of these scans was an attempt to image the dopant profile of the sources/drains and the LDD regions, but several other features of interest to FA were also imaged.

This particular sample was prepared with a 30 minute dip in buffered HF at IBM – Essex Junction. The sample was sent to Dartmouth College, mounted, and examined with the SKPM without further processing. Thus, we are imaging surface features through a thin layer of native oxide and possibly a film of water.

The lighter contrast regions in both images of Figure 6 correspond to the channels of two adjacent n-channel MOSFETs, and the darker regions are the sources/drains. The dark spots imaged in the sources/drains are remnants of the vias. The surfaces in the EPD image are much rougher than in the vdW image, which we believe is due to variations in dopant density. The sources/drains are clearly distinct from the channels in both images, with the EPD signal showing a wider transition due to the lateral diffusion of the dopants. The EPD signal also shows a step in

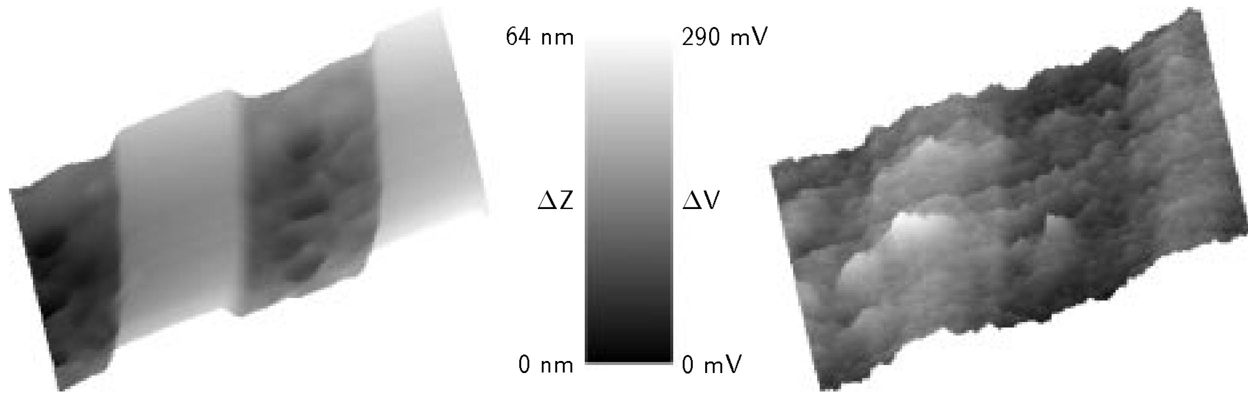

Figure 6: vdW (left) and EPD (right) images from a 5 μm $\times$ 5 μm scan of n-channel MOSFETs.

the transition region that is not seen in the vdW signal, which we attribute to the LDD profile.

Two anomalies may be clearly seen in the EPD signal of the left n-channel that have no corresponding vdW features. Figures 7 and 8 show profiles of the normalized vdW and EPD measurements. The horizontal line in Figure 7 indicates the mean value of the EPD signal in the channel, not including the defect regions. The lateral extent of the defect region is three-quarters of the channel width, and extends into the source/drain. The magnitude of the EPD signal associated with this defect indicates that the local WFD between the gate and channel for this device would lead to large variations in the channel mobility. The exact nature of these anomalies is not known, but we believe that the two most likely causes are excess dopant in the channel region or a change in the density of surface states.

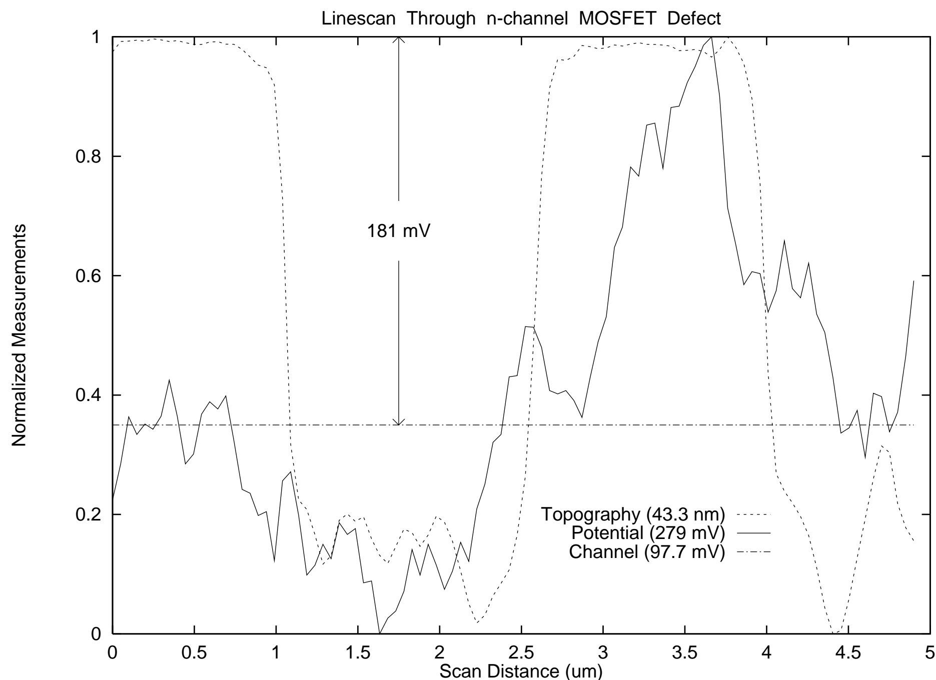

Figure 7: Line profiles of the normalized vdW and EPD measurements shown in Figure 6 taken parallel to the direction of the scan and through the strongest n-channel defect. The values in parentheses are the full scale changes of the normalized signals.

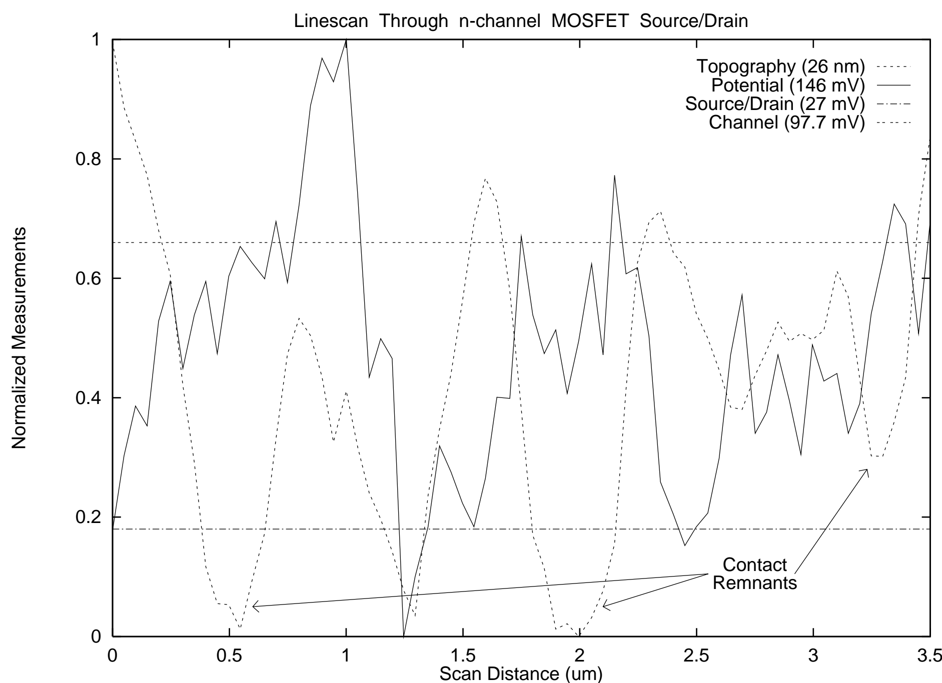

Figure 8: Line profiles of the normalized vdW and EPD measurements shown in Figure 6 taken perpendicular to the direction of the scan and through the via remnants. The values in parentheses are the full scale changes of the normalized signals.

A second feature of interest in the EPD measurements is the impact of the via remnants. The plot in Figure 8 shows the normalized vdW and EPD signals in the area of the vias. It shows that the EPD signal of the via remnants is at a similar level as the mean channel EPD level. The most likely causes for this are stress, dopant displacement, or deep-level impurity states from metal/silicide impurities. It is unlikely that the via went completely through the junction since the depth of the remnants is much smaller than the expected junction thickness.

4 Conclusion

We have demonstrated that the SKPM is a viable tool for FA on devices well into the sub-micron size range. The functionality of an SKPM may be added to any non-contact AFM at minimal cost, and measurements may be done in a lab or fabrication line environment. Sample preparation can be minimal, although standard cleans will probably be required for future quantitative results. The small probe size and non-contact nature of the technique allows us to obtain electrical measurements without the need of large probing pads, and to examine material properties on a scale much smaller than minimum feature sizes. Future research includes applying the technique to devices under bias and the formulation of a robust technique to extract a quantitative WFD and capacitance variation from the EPD and $\frac{\partial C}{\partial z}$ measurements.

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