reversed and positive charge trapping is obtained [3]. This behavior suggest that the first order model is not valid for the 10^{-16} cm^2 cross section traps. We show that these results can be described by a unified dynamic trapping-detrapping model, which explains the continuous transistion from low-field electron trapping to high-field positive charge generation.

It is also shown that much of the measured slow build-up of oxide charge is due to generation of new traps with $\omega \sim 10^{-16}$ cm^2. The oxide charge trapping dynamics is limited in this case by the trap generation rate and not by the trapping cross section, as is assumed in the conventional model.

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IVB-4 Characterization and Two-Dimensional Simulation of Impact Ionization Current in MOSFET's Between 77 and 300 K—Albert K. Henning and James D. Plummer, Department of Electrical Engineering, Stanford University, Stanford, CA, and Nelson Chan, Intel Corporation, Santa Clara, CA.

Silicon is the material of choice for fabrication of high circuit density, low defect density, and high-speed integrated devices. CMOS technology provides the additional advantage of low power dissipation. Performance enhancement can be obtained by operating CMOS circuits at liquid nitrogen temperatures [1]. However, low-temperature operation exacerbates the generation of substrate current by impact ionization in n-channel transistors, leading to potential device degradation [2]. This work characterizes the temperature behavior of the substrate current, and presents a model describing this behavior based on Shockley's lucky electron (LE) model [3], and a Maxwell–Boltzmann (MB) distribution of hot-electron energies above the conduction band minimum. We implement the model in the 2-D device simulator CADDET [4]. The model succeeds in explaining the observed substrate current over a wide range of temperature, gate voltage, and drain voltage.

CMOS transistors were frabricated at the Stanford IC Lab using a conventional n-well process, with $T_{ox} = 385$ Å. n-channel devices were measured, with $1 \leq L_e \leq 25$ μ. R_{eox} encroachment of 0.17 μm per source–drain edge was determined by electrical measurements, and led to a slightly nonuniform oxide thickness over the electrical channel, which was incorporated later in the CADDET simulation. Low V_D transconductance and V_T were monitored before and after I_V measurements at each temperature, to ensure the measurements did not degrade the device. Substrate current I_B was measured for $0 < V_G < 5$ V, $1.6 < V_D < 5$ V and $77 < T < 300$ K.

Previously, an LE model has been used successfully to model I_B [6], as well as other NMOS effects [7]. One drawback of this model was its inability to predict I_B accurately over a wide range of V_G and V_D. This work uses an MB distribution function to augment the previous model. Use of the MB model allows correct prediction of the shape of I_B versus V_G over nearly all V_G and V_D ranges; in addition, this model predicts the correct temperature dependence of I_{Bmax}/I_D—which cannot be done with either a simple LE model of a model incorporating energy contributions from the lattice [5]. The modified version of CADDET follows and extends the models of [6], with the resulting rate equation

$$R_{ii} \sim J_D \exp\left(-\frac{x_{ji}}{\lambda_T}\right)\left\{\left(\frac{E_g - V_{ji}}{kT_e}\right)\exp\left[-\frac{(E_g - V_{ji})}{kT_e}\right]\right\}.$$

J_D is the current density along the path. λ_T is the total scattering mean free path. E_g represents the energy required to break a Si–Si bond. V_{ji} is the energy gained by an electron transversing the path between i, and j, $x_j - x_i = x_{ji}$. The first exponential represents the lucky electron probability, while the factor in braces represents the probability of a hot electron having the required energy to cause an impact ionization event. The electron temperature T_e [8] specifies the MB distribution.

Simulation results for the full I_B versus V_G curve for low and moderate V_D show the LE model alone is insufficient to explain the behavior at high V_G over the whole V_D range, while the enhancement of the MB model allows close estimation of the full curve shape. The T dependence of I_{Bmax} is simulated and compared with the measured results, confirming that an LE model, alone, fails to give a quantitative explanation of the observations, especially for low V_D.

The data demonstrate that substrate current can be held constant, or perhaps even reduced, by proper scaling of power supply voltage for a CMOS technology optimized for liquid nitrogen operation. This effect is a field, not voltage, effect, as pointed out in [5] and modeled with good success in this work. However, the field effect here is modeled using both an LE probability (not an ionization coefficient following Chynoweth's derivation) as well as an MB distribution for electron energies above E_c, which is determined by a field-dependent electron temperature. In addition, the LE model does not require any assumption of constant field. However, comparison with the device characterized in [5] indicates the maximum power supply voltage to keep I_B constant in submicrometer devices for use at liquid-nitrogen temperatures may be less than that which can be tolerated for noise considerations—despite the low noise and sharp on-off characteristics at such reduced temperature.

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IVB-5 Degradation Behavior of Dynamically Stressed N-MOSFET's—W. Weber, Siemens AG, ZT ZFE ME 31. Otto-Hahn-Ring 6, D-8000 München 83, West Germany.

Dynamic degradation experiments have been performed in which various pulse configurations were applied at n-MOSFET's with different endpassivations.

A first comparison between static and dynamic degradation results has been reported in [1] which showed an enhancement of the dynamic over the static degradation by up to a factor of 4 for nitride passivated samples. In this paper the experimental basis is extended and the results are discussed in the framework of a model proposed for static degradation [2].

Dynamic stress experiments were performed at transistors with nitride (N), nitride + oxide (N + O), and without passivation by applying separate pulses at gate and drain. The pulse overlaps were varied from non- to completely overlapping configurations. The degradation for different amplitudes of the gatepulse was compared with corresponding static degradation results.

For samples with different endpassivations we got the following results for complete overlap of gate- and drain-pulse: (N + O) and unpassivated samples show similar degradation results which are quantitatively different from and about a factor of 10 lower than those of (N) samples. Furthermore, the differences between static and dynamic degradation results are much smaller in the (N + O)