Imaging integrated circuit dopant profiles with the force-based scanning Kelvin probe microscope

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A force-based scanning Kelvin probe microscope has been used to image dopant profiles in silicon for integrated circuit devices on a submicron scale. By measuring the potential difference which minimizes the electrostatic force between a probe and surface of a sample, an estimate of the work function difference between the probe and surface may be made. To the extent that this work function difference is a consequence of the dopant concentration near the sample surface, doping profiles are inferred from the measurements. An overview of the measurement technique is presented, along with several examples of resulting dopant imaging of integrated circuits. © *1996 American Vacuum Society.*

I. INTRODUCTION

Previous experimental results have shown that the simultaneous use of an atomic force microscope (AFM) and scanning Kelvin probe force microscope (SKPM) can provide qualitative dopant concentration profiles in simple structures.[1–7] This work presents the use of the SKPM in determining positions of dopants, or missing dopants, from actual integrated circuit devices.

A brief description of the measurement technique will be presented, followed by a discussion of the following measurements that focus on problems of technological interest: analyzing bipolar device failure due to a missing p-well implant; determining implanted metal–oxide–semiconductor field-effect transistor (MOSFET) channel length dependence upon wafer orientation; measuring the presence of anomalous dopants in the channels of complementary metal–oxide–semiconductor (CMOS) gates; and imaging lightly doped drain (LDD) structures in n-channel MOSFETs.

II. MEASUREMENT SYSTEM

Our force-based SKPM is developed upon a noncontact AFM originally built at IBM's Thomas J. Watson Research Center.[8] The necessary electronics have been added to convert the system to the force-based SKPM.[9] Details of the operation may be found in Ref. 6, and details about the nature of the electrostatic force may be found elsewhere.[10–14] In this section only the information necessary to understand the origin of the measurements discussed in this article is presented.

As a result of an applied electrical bias between a force-sensing probe and the surface of a sample, the cantilever of the probe will deflect. The deflection will depend upon the voltages involved and the material properties of the probe and sample. By monitoring the amount of deflection, these properties may be inferred. Due to the nature of the electrostatic force, the cantilever will experience at least two modes of vibration. These modes yield signals proportional to

$$S_{\omega} \propto \left(\frac{C_{\mathrm{eff}}}{C_{\mathrm{air}}}\right)^2 \frac{\partial C_{\mathrm{air}}}{\partial z} \left(V_{\mathrm{dc}} - \frac{\Delta\Phi}{q}\right) V_{\mathrm{ac}} \sin(\omega t), \tag{1}$$

$$S_{2\omega} \propto \frac{1}{4} \left(\frac{C_{\mathrm{eff}}}{C_{\mathrm{air}}}\right)^2 \frac{\partial C_{\mathrm{air}}}{\partial z} V_{\mathrm{ac}}^2 \cos(2\omega t), \tag{2}$$

where z is the spatial distance; C_{air} is the capacitance—and $\partial C_{\mathrm{air}}/\partial z$ is the spatial derivative of this capacitance—between the probe and sample; C_{eff} is the total capacitive load in series with the system, including contributions from the probe/sample gap, dielectric materials on probe or sample surfaces, and bulk p/n junctions in the sample; V_{dc} is the magnitude of the dc component applied by any external electronics; $\Delta\Phi$ is the work function difference (WFD) (in eV) between the probe and surface materials [and $\Delta\Phi/q$ is the contact potential difference (CPD)]; V_{ac} is the peak magnitude of the ac component of the externally applied potential between the probe and the sample; ω is the frequency at which the ac voltage is oscillating.

A compensating V_{dc} is applied to minimize the signal of Eq. (1). Since the capacitance and V_{ac} terms of this equation are nonzero, the deflection is ideally minimized when the applied voltage is equal to the CPD of the materials. In practice structural, compositional, and charge inhomogeneities near the probe result in the value of V_{dc} differing from the true CPD.

A lock-in amplifier is used to track the signal of Eq. (2). This yields information about the spatial variations in the capacitance between the probe/sample electrodes. It provides additional information unavailable using only the Kelvin loop. As shown in Ref. 12, this mode will be important for obtaining quantitative results from SKPM measurements.

The feedback voltages and magnitude of the detected voltages associated with these signals are acquired with a separate computer and stored for later processing. In this

article references to the various measurements are as follows: topography-related data are the van der Waals (vdW) signal (in practice there may be contributions to the attractive-force topography signal from forces in addition to the van der Waals force, notably capillary force from surface moisture); the value of V_{dc} is the electrochemical potential difference (EPD) signal; and the magnitude of Eq. (2) is C'.

The system consistently achieves lateral resolutions under 100 nm, a closed loop vdW noise level of 0.5 $Å/\sqrt{Hz}$ measured in a 100 Hz bandwidth, and a closed loop EPD noise level of $5 mV/\sqrt{Hz}$ measured in a 160 Hz bandwidth. The system has achieved lateral resolutions of 25 nm, a closed loop vdW noise level of 0.1 $Å/\sqrt{Hz}$, and a closed loop EPD noise level of $1 mV/\sqrt{Hz}$. The SKPM is run with a 100 Hz bandwidth for the vdW loop, and 20–30 Hz bandwidth for the EPD loop. As mentioned in Ref. 6, under ideal circumstances that ignore nonlocalized capacitance effects, an EPD noise level of $1 mV/\sqrt{Hz}$ translates to an estimated sensitivity to changes in actual dopant concentration of $\pm\ 5\%/\sqrt{Hz}$ in the vicinity of $10^{14}\ cm^{-3}$, and $\pm\ 8\%/\sqrt{Hz}$ in the vicinity of $10^{18}\ cm^{-3}$.

The SKPM has been used to image p- and n-type structures over the range of $10^{14}\ cm^{-3}$–$10^{20}\ cm^{-3}$. The range of the measured signal depends strongly upon the structure being examined and the settings of the feedback loop, so in practice the operational sensivity varies. For the study examining the bipolar structure, the sensitivity was $\pm 12.5\%$ for $10^{16}\ cm^{-3}$ and $\pm 17\%$ for $10^{19}\ cm^{-3}$. For the imaging of the transistor cross section, the signal swing was reduced due to the small size of the device relative to the probe. Thus, the noise was a larger fraction of the signal, and the sensitivity is estimated to be $\pm 30\%$ for $10^{17}\ cm^{-3}$.

The resulting measurements may be analyzed quickly to yield qualitative information about the sample. For quantitative measurements, it is necessary to perform deconvolution of the data. To successfully deconvolve the data, the probe/sample system must be modeled as accurately as possible. This process is lengthy in terms of generating the models and in performing the deconvolution, and more work needs to be done to understand the nature of the probe/sample interaction before the extracted data can be called quantitative. No deconvolution has been performed on any of the measurements in the following sections. Most of the data is in raw form, with any modifications indicated on the corresponding figures or text.

III. MISSING *p*-TYPE IMPLANT

The SKPM has been used to determine if the fabrication process of a bipolar device missed the implant of p-type dopants. For these measurements, two separate die were scanned. Both were etched chemically to remove all upper dielectric and metal layers. They were rinsed with deionized water, mounted, and scanned in various areas over a three day period. The results shown here were taken on the same day.

Figure 1 shows the EPD result of one set of scans from the functional and failing samples. The profiles are averages

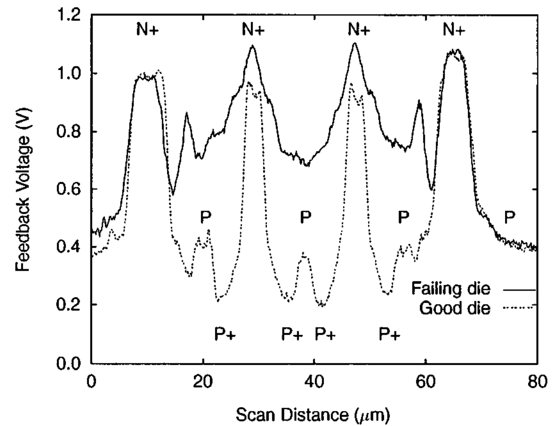

FIG. 1. Averages of nine scan lines from EPD measurements of a bipolar device fabricated with a CMOS process. One die did not receive any p-type implants, which shows up clearly when compared to a device that did receive all implants. The measurements show excellent consistency in areas common to both die.

of nine measurements along the scan lines, which were taken over a 10 μm area. The missing p-type implant shows up very clearly when compared to a correctly processed sample. The potentials associated with the p-type background and outermost n^+ implant show excellent consistency between the two samples. The potential in the interior surface region of the failing die does not drop back below the potential of the p-type substrate since it never received the p and p^+ implants.

There are two subtle features of these profiles. For the good sample (the dotted line in Fig. 1), there is a p-type region between the p^+ and n^+ regions, which shows up as a change in the spatial slope of the potential. Unlike the outermost n^+ regions common to both samples, the innermost n^+ regions do not yield the same potential. This effect may be due in part to the compensating p-type implant, but it is mostly due to undesired capacitive coupling between the sample and cantilever of the probe as described in Ref. 12.

IV. CHANNEL LENGTHS

The SKPM has been used to examine the impact of mask/wafer orientation on MOSFET effective channel lengths. In this study, two wafers were processed. One was aligned with the mask along the ⟨100⟩ direction, and the other along the ⟨110⟩ direction. After processing, samples were extracted from the wafers and etched chemically to remove the gates and oxide. The samples were mounted, and several transistors of different sizes were examined on each sample. Here the results for transistors with channel lengths of 5, 2, and 1.3 μm are presented.

Ideally, a direct comparison of the data from the scans would be made. Unfortunately, in our system variations in sample mounting lead to differences in the scans from sample to sample. As shown in Fig. 2, the effective scan line lengths then differ from sample to sample, and corrections for these angular differences in the scans need to be made. The software controlling the motion of the scanner does not

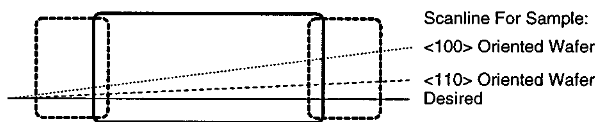

FIG. 2. Schematic representation of the probe/sample orientation, and the resulting scans, discussed in the text. The solid line is the ideal scan line for both samples. In practice, sample mounting variations lead to scans shown as the dotted (⟨100⟩ oriented MOSFET) and dashed lines (⟨110⟩ oriented MOSFET).

allow us to adjust the direction of the scans, so corrections must be made after the data have been acquired. In this case several features on all sets of scans were examined, and the lateral rotation needed to return the surface features to horizontal and vertical orientations was determined.

The vdW images of devices from the ⟨100⟩ sample needed to be rotated by an angle that was 14°–17° larger than that required for images of the ⟨110⟩ sample. Because the vdW images need to be rotated by different angles, the distance between the physical edges of the channel on a single scan line is not the same between samples. Individual vdW line profiles indicate that the distance between the measured edges of the device channels on the ⟨110⟩ sample was consistently between 94.7% and 96.6% of that for devices on the ⟨100⟩ sample. If a mean value of 15.5° is used for the difference in lateral probe/surface orientation of the samples, then simple trigonometric relationships indicate that the effective scan distance for one sample will be slightly less than cos(15.5°), or 96.4%, as large as the scan distance on the other sample if the features are the same size on both samples. Thus, the angular correction and spatial distances are consistent for the samples examined. This indicates that the etching did not alter the surface features as measured with the vdW mode.

Because of this consistency, the ratio of the lateral size of the EPD to the vdW signal on the two samples may be compared, which does not require an exact correction for the probe/sample orientation. However, similar comparison criteria must be used for each transistor. The vdW measurement was taken to be the distance between the first two points found at -20 nm from the mean value of the channel—in Fig. 3 these points are at 0.32 and 3.29 μm. For the EPD signal the length was chosen to be the distance between the points near the middle values of the full-scale swing in measurement potential (similar in spirit to full width at half-magnitude measurements). As seen in Fig. 3 these points do not necessarily have the same values on either end of the channel.

Figure 3 shows the vdW and EPD measurements from a single scan line of a 2 μm transistor. The vdW images have been corrected for a background slope in the scan along the surface of the channel. The ⟨100⟩ sample has been scaled laterally by 96.1% in order to correct for the differing scan orientations (as described above). The vdW image shows that the shape of the surface on either side of the channel region is the same for the two samples. This indicates the vertical orientation of the tip relative to each sample was nearly identical. The EPD scan of the 2 μm transistor clearly shows that the electrical signals have very different lateral extents. This difference was also found for the 5 and 1.3 μm transistors.

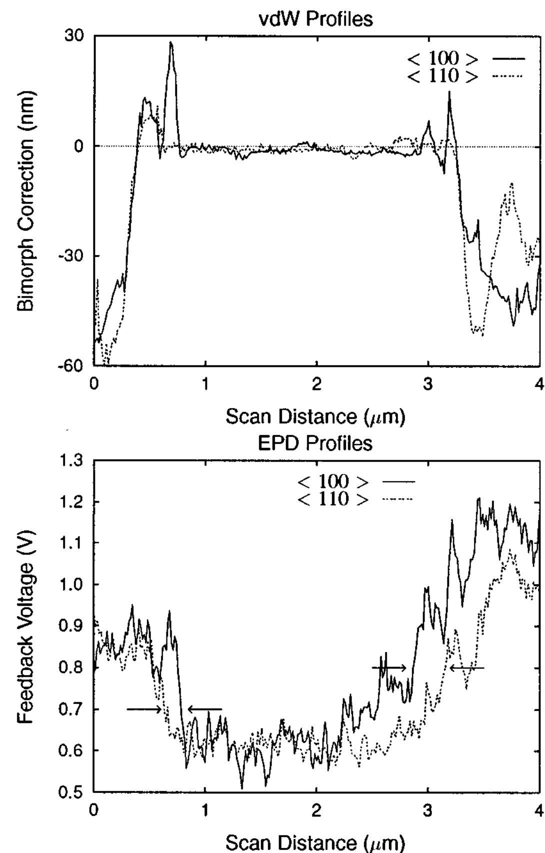

FIG. 3. Single scan lines of vdW and EPD measurements from initial examinations of n-type channel length variations due to mask/wafer orientation. The profiles shown here are for transistors with channel lengths of 2 μm. The measurements have been corrected for differing probe/sample orientations (see the text).

Due to the small sample population used so far in these studies, it is necessary to consider the statistical certainty of our measurements. Table I shows the ratios of the EPD to vdW measurements, and the channel length variations for a given confidence level. The measurements analyzed to date show a 75% confidence that the 5 μm transistor channel length on the ⟨110⟩ wafer is 4.77% larger than for the ⟨100⟩ wafer, and a 95% confidence that the difference is 4.09%. The values for both the 5 and 2 μm transistors are close, but the 1.3 μm is much worse. This is probably due to the device approaching a size that is only an order of magnitude larger than the probe tip size. The results of these scans are consistent with electrical measurements which first indicated a difference in the devices.

V. ANOMALOUS CHANNEL DOPANTS

The scans discussed in this section are from a CMOS memory chip, and represent our first attempts to apply the SKPM to dopant imaging in fully processed integrated cir-

TABLE I. Statistical analysis of the effective channel length in the devices studied to date.

Transistor size	⟨100⟩ EPD/vdW ratio	⟨110⟩ EPD/vdW ratio	The amount that the ⟨110⟩ channel is larger than the ⟨100⟩ channel for the specified confidence level			
			60%	75%	90%	95%
5 μm	0.903±0.020	0.955±0.023	0.0504	0.0477	0.0436	0.0409
2 μm	0.890±0.044	0.944±0.036	0.0498	0.0426	0.0315	0.0241
1.3 μm	0.924±0.046	0.948±0.046	0.0199	0.0130	0.00236	−0.00458

cuit devices. All dielectric and metal layers have been removed chemically from the sample, leaving behind the substrate and poly-silicon gates.

The primary goal for analysis on the sample was to determine if dopants had been implanted through the poly-silicon gates and into the channel. If dopants were in the channel or the gate oxide was defective, the surface nature of the EPD signal would show very little difference between the functional and failing gates. On the other hand, the C' signal should show differences since it depends upon the total region between the electrical connections to the probe and backside of the sample.[2]

Figure 4 shows two different line profiles from measurements made on different failing areas of the same sample. The profiles show two adjacent devices, one of which failed the electrical measurements. The profiles are taken perpendicular to the scanning direction, with the left edges of the graphs lying along the first scan line.

The vdW measurements do not indicate significant differences between the physical shape of the devices, which rules out variations in gate oxide or poly-silicon thickness as the source of failure. The EPD measurements show comparable signal swings over failing and functioning devices, indicating similar surface conditions for both devices.

However, the C' signals indicate a difference between the two gates. The relative variations are consistent in the two measurements shown here, and were found to be consistent in other failure areas on the same sample. This change in contrast was also consistent with electrical and TEM measurements made on the gates at IBM—Essex Junction.[15]

There is some structure in the C' signal between the gates that should be addressed. The regions between the gates are the doped sources and drains. There was topographical structure on the surface of the source/drain regions due to removal of the silicide and metal contacts. The variations in the C' signal in these regions are correlated to the topographical variations, and possibly indicate dopant displacement or residual silicide.

The EPD signal shows smaller peaks which are seen on either side of the gates. The C' signal shows valleys on either side of the gates. These features are due to lateral capacitance effects[12,16] and the presence of LDD structures.

VI. LDD IMAGING

The imaging of LDD structures in planar scans has already been reported elsewhere.[6] More measurements have been made on devices fabricated with LDD structures, and these recent scans are presented here. Figure 5(a) shows a schematic of the planar scans of n-channel MOSFETs. The sample consisted of adjacent MOSFETs fabricated with LDD structures. The sample was etched chemically in order to remove all material from the silicon surface, including the poly-silicon gates and gate oxide.

Figure 5(b) shows the ideal shape of the substrate energy bands near the surface. Figure 5(c) indicates the expected shape of the feedback voltage necessary to minimize Eq. (1) for the energy band profile. When the probe is grounded and the feedback bias is applied to the substrate, the CPD be-

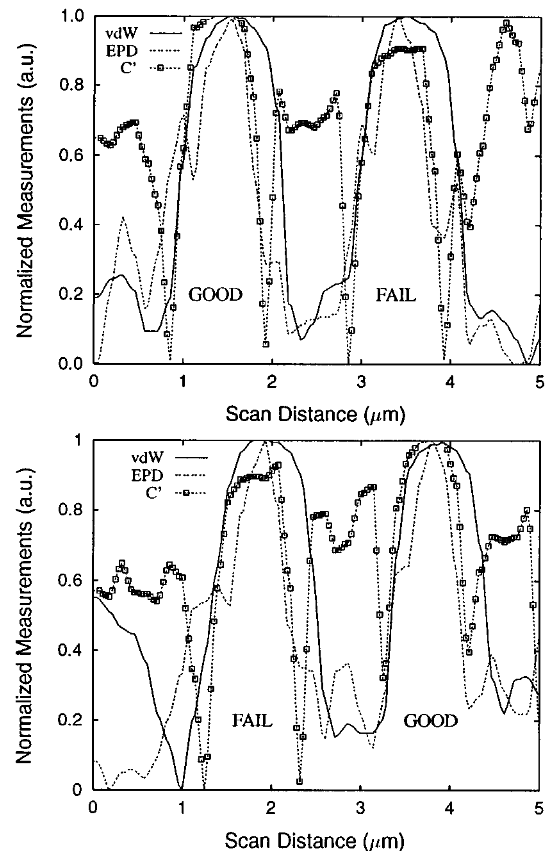

FIG. 4. Line profiles of adjacent CMOS gates, taken perpendicular to the scan direction. The measurements have been normalized to fit on one graph. Both a failing (fail) and functioning (good) device are shown in each profile. The failure signature is strongest in the C' signal, indicating the mechanism is beneath the surface (see the text).

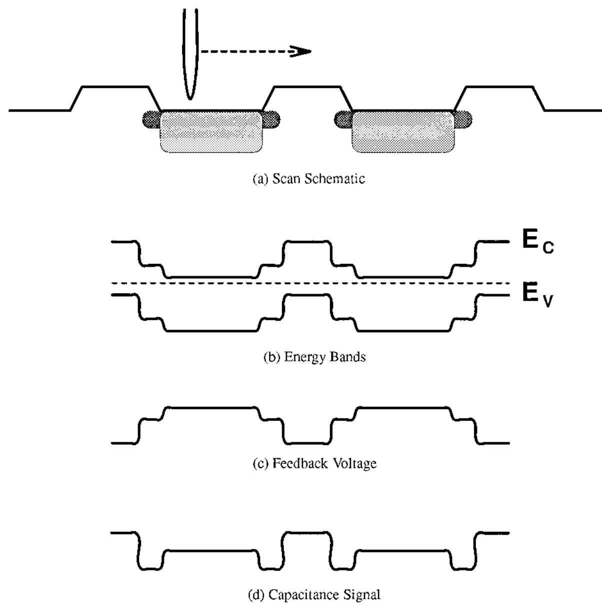

FIG. 5. Schematics for the imaging of LDD in planar structures.

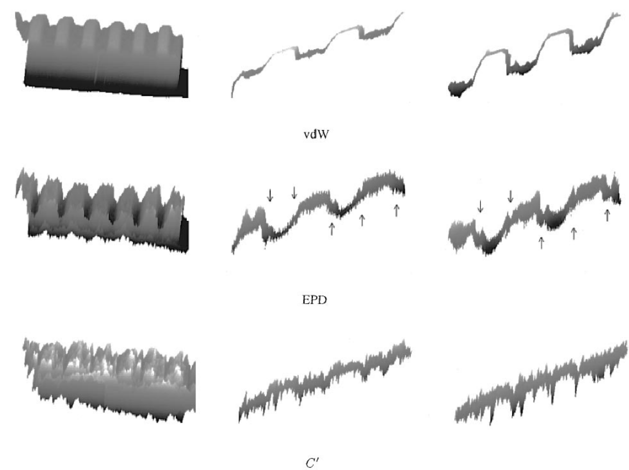

FIG. 6. Shaded surface images from planar scans of n-channel MOSFETs. The middle and right-hand columns of images are from higher resolution scans of the devices seen on the left-hand side. The channel regions are smooth and light in the vdW images, and darker in the EPD images. The LDD may be seen as a step in the transition between channel and source/drain of the EPD signal. The slope seen in the figures is an artifact of the shading process, and is not present in the actual EPD and C' data. The LDD regions are indicated by the arrows.

tween the sample/probe for n-type material is positive relative to the CPD of p-type material, so the feedback voltage for the source/drain regions will be larger in value than for the channel.

Figure 5(d) shows the expected shape of the C' signal for the situation where Eq. (1) has been minimized. Assuming a p-type background of 10^{17} cm^{-3}, simple formulas[17] indicate that as the n-type density increases from 10^{17} to 10^{19} cm^{-3} the effective thickness of the depletion region decreases. A thinner depletion region implies a larger substrate capacitance, so the LDD region should yield a lower measured capacitive value than the source/drain. The effective capacitance over the channel region depends strongly upon the probe/sample interaction. For a probe/sample spacing of 10 nm simple capacitance models indicate it is roughly twice as large as the source/drain junction capacitance.

Figure 6 shows shaded surface images from planar scans of the n-channel MOSFETs. The left-hand column shows a coarse 20 μm scan of the edge of an array of transistors, and the other two columns are 8 μm scans of interior regions of the array.

The top row of images shows vdW measurements. The smooth, light areas correspond to the channel regions. The rough, darker areas correspond to the source/drain. The slope on either side of the channel is different due to the sample and probe not being perfectly parallel. The vdW images show very abrupt changes at these display scales, but there is a slight topographical feature from the sidewall spacer used during fabrication of the devices.

The middle row of images shows the EPD measurements. The n^+-type sources/drains appear as the lighter regions, which correspond to higher probe voltages. The p-type channel appears as the darker sections, which correspond to lower feedback voltages. In the transition region, there is clearly a step imaged in the potentials, which corresponds very well with the intended placement of LDD in device fabrication.

The bottom row of images shows the C' measurements. Here, there appear to be three distinct voltages related to the different capacitances. The channels are lightest, indicating a larger effective probe/sample capacitance. The sources/drains show up as slightly darker, indicating a lower effective capacitance. As in the previous measurements the LDD regions show up as the sharply defined valleys, indicating an even lower effective capacitance than in the other regions. Thus, our measurements are qualitatively consistent with the expected behavior described above.

There appear to be smaller peaks in the C' images along the source/drain and channel regions. Since only the magnitude of Eq. (2) is measured, there is more noise in the C' images than in the EPD images. The C' variations along the channels are mostly due to this noise. The fluctuations imaged in the source/drain regions are larger than in the channels. As with the previous study, the variations in the source/drain regions may be partly due to displaced dopants or residual silicide.

Transistor cross sections have also been examined. The scans of cross sections are much more difficult than planar scans due to problems with scanning off the edge of the sample and positioning the probe tip near the area of interest. The full signal swing of the EPD loop is greatly reduced from theoretical values due to the small lateral size of the dopant implants relative to the probe size. Thus, it is difficult to extract electrical features from noise unless the control loops are set properly.

Figure 7 shows a schematic of and measurements from the scan of a transistor cross section. The dotted lines labeled A, B, C, and D in the schematic roughly correspond to the line profiles shown in the graph. The origin of each scan line

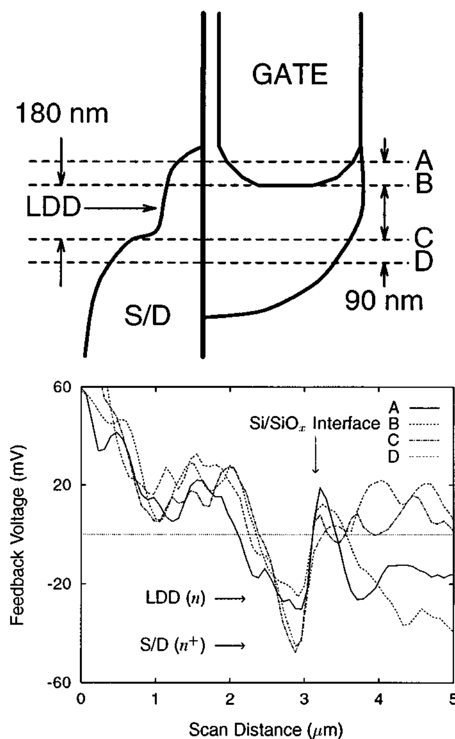

FIG. 7. Schematic and measurements of a cross-sectional scan showing the imaging of LDD. The schematic shows the area of the device that was scanned. The graph shows the measurements along four scan lines, which clearly indicates two distinct potentials in the source/drain region of the transistor. The scan lines have been corrected for the probe/sample orientation.

lies over the substrate, and the end of each scan line lies over either the gate or oxide. The electrical connections to the probe and sample are reversed from the previous scans shown, so the resulting signal levels of the n- and p-type materials also change.

The measurements indicate two distinct potentials in the silicon near the Si/SiO_x interface. The potential is lowest when the probe scans over the source/drain, and it is slightly higher when scanning over the LDD region. The potential on the oxide/gate side of the interface begins to drop as the probe enters the LDD region, consistent with the n-type doping of the gate.

VII. CONCLUSION

These measurements of dopants, in addition to failure analysis measurements from other devices of technological interest,[18–20] indicate that the SKPM is a viable tool for use in material studies of silicon-based devices. The functionality of a force-based SKPM may be added to, or is already available on, noncontact AFMs. The measurements may be performed in a lab or fabrication line environment.

Sample preparation can be minimal, although standard cleaning procedures will likely be necessary for successful quantitative results. The technique has a lateral resolution well into the submicron range, and is sensitive to electrical signatures on the mV level. The small probe size and noncontact nature of the technique allow us to obtain electrical measurements without damaging or perturbing the sample under test.

The measurements performed on anomalous channel dopants presented in this article, substrate fractures in Ref. 18, and ionic contamination in Ref. 19, indicate that the SKPM is suitable for simultaneous imaging of the surface and bulk nature of possible defects. The EPD signal is most sensitive to variations in the surface of the sample. The C' signal is sensitive to the entire electrical signal path, and can yield information about bulk defects. By examining both sets of information, the vertical extent of the electrical defect into the sample may be determined.

Results to date have been mostly qualitative in nature. Research is underway to reach a better understanding of the nature of the electrostatic force in order to formulate a robust technique to extract quantitative information from measurement data. This will involve the use of known dopant structures and available TCAD tools as described in Ref. 6 in addition to the use of production-level devices as shown here.

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