Modified ELTRAN® - A Game Changer for Monolithic 3D

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***Abstract* — It is well recognized that dimensional scaling has reached its diminishing return phase and the industry is now looking to monolithic 3D to be the future technology driver. This was clearly voiced in the Qualcomm keynote at DAC 2014 and follow-on presentation at ISPD 2015. This paper will present a novel use of the ELTRAN® process developed by Canon Inc. about 20 years ago primarily for SOI applications. Using ELTRAN techniques, a substrate could be prepared enabling any fab to simply integrate a monolithic 3D device without the need to change the current frontline fab process. This flow is further simplified and could be integrated with the game changing monolithic 3D flow introduced last year which leverages the emerging precision bonders, such as EVG's Gemini® XT FB. This flow provides a natural path for product innovation and an unparalleled competitive edge. In addition, this game-changer breakthrough offers a very cost competitive flow.**

Introduction

For many years monolithic 3D was considered untenable due to the strict 400 ºC temperature limit imposed by the underlying aluminum or copper interconnect. This led to the focus on TSV technology as the only viable path for 3D ICs. Unfortunately, it is now clear that the TSV flow is intrinsically expensive and accordingly being perpetually pushed to the future. In recent years pioneering efforts have been published providing practical paths for monolithic 3D logic devices [1-7]. But each and every one of those presented new transistor formation flows and comes along with additional non-trivial process development challenges.

Last year we introduced [8] a game-changing flow leveraging the new class of precision bonders [9, 10]. This paper proposes a process flow that leverages an alternative for the ion-cut process, thus overcoming some limitations associated with ion-cut and further reducing the cost and simplifying the integration of a monolithic 3D flow within existing fab lines. This flow provides a true monolithic 3D IC without the need for a new recipe for transistor formation. The process could be adopted by any current fab and provides very competitive costs for a range of product enhancements as well as a long term road map for better offerings by scaling up.

ELTRAN - A Layer Transfer Technology

About the same time Soitec developed the ion-cut process for the fabrication of SOI wafers, an alternative process was developed by Canon Inc. [11, 12, 13]. This process was named ELTRAN and is illustrated in Fig. 1. The starting step is a wet etch step under anodizing current forming a porous silicon layer at the upper surface of a donor wafer. High temperature H_2 annealing is then used to seal the top surface and is followed by epitaxial growth of a COP (Crystal Originated Pits) free monocrystalline layer on top of the porous layer. A thin oxide for bonding is then grown on top. The donor wafer is then bonded to the target wafer. Using a water jet the porous layer is cut, thereby lifting off the donor wafer which is sent for rework and reuse. The thin epitaxial layer is left bonded on top of oxide of the target wafer. The residues of the porous layer are removed by highly selective etching ($>10^5$), and H_2 annealing is used to form an atomically flat top surface.

Monolithic 3D IC

The key for this new flow is that wafers pre-processed for ELTRAN layer transfer, such as illustrated in Fig. 2 and Fig. 3, could be used for normal front-line processing with its associated high temperature steps. The early work by IBM [15, 16] and Intel [19], collaborative work of Canon and Stanford University [14], and ongoing work by IMS Chip [17, 18] all validate this feature. A substrate provider could prepare two types of wafers—Donor Wafer (Fig. 2) and Carrier Wafer (Fig. 3)—ready for future cuts. All the additional equipment needed for the fab to integrate a monolithic 3D flow would then be a simple wafer bonder, a 'water jet porous wafer cutter', and supply of these special substrates. Fig. 4 A-I illustrates this modified ELTRAN monolithic 3D flow.

Fig. 4A illustrates the donor wafer after being processed through standard front-line processing to form the first transistor layer – Stratum-3.

Fig. 4B illustrates the donor wafer flipped and bonded on top of the carrier wafer. The bonding step is simple without a precision alignment requirement as it is bonded to a generic un-patterned carrier wafer.

Fig. 4C illustrates cutting the donor wafer off using the water jet to cut-off the pre-processed porous layer. The selective water jet splitting could be done by changing the porosity as well as the number of porous silicon layers between the donor and carrier structures. The residue of the porous structure could be etched away using a solution containing a mixture of HF, H_2O_2 and H_2O. Once a certain incubation period has passed, the porous silicon is etched virtually all at once, as the selectivity of this etching is as high as 100,000:1, meaning that the etching does not cause significant thickness uniformity degradation of the remaining layer [11]. It also means that the Donor Wafer could be recycled for reuse, and the transferred layer is now ready for future processing as is illustrated in Fig. 4D. In addition to the removal of the porous layer by etch, a hydrogen annealing could be used to further smooth the top layer surface. There is no need for expensive CMP processing or ion damage repair as would have been required for an ion-cut.

Fig. 4E illustrates the wafer after adding local interconnects. These local interconnects are optional and should use high temperature metal such as tungsten. These interconnects could support both Stratum-3 and the coming

Stratum-2. It could also carry the power distribution network (PDN) for both strata and assist heat removal.

Fig. 4F illustrates a layer transfer step. This layer transfer could use an ion-cut or ELTRAN process; as high temperatures are acceptable at this phase.

Fig. 4G illustrates a second front-line processing to form Stratum-2 (after the completion of the layer transfer). The second front-line processing could be again done by a standard transistor flow as the wafer at this point does not have any copper or aluminum interconnection which would limit the front line process flexibility. Stratum-2 could be precisely aligned to Stratum-3. The same alignment marks could be used for both strata processed, as the layer is very thin and alignment marks can be easily seen from both sides.

Now the interconnection layers for Stratum-2 can be processed as illustrated in Fig. 4H. For some applications, such as an image sensor device, this could be the end of the fab process.

For many other applications there would be a need for adding interconnection to Stratum-3 as illustrated in Fig. 4I and 4J. The carrier wafer could also be sent back for recycling, thus further reducing the overall cost.

For a more than two-stratum 3D device, a Precision Bonder could be used. In such case the final carrier illustrated in Fig. 4I as a target wafer would be replaced with a target wafer using a precise bonder, for precise alignment over Stratum-1. The bonding could be a hybrid bonding forming the connection to Stratum-1, or an oxide to oxide bonding allowing 'smart-alignment' as was presented elsewhere [8].

Monolithic 3D Cost Estimates

It is well known that high cost is the number one issue which has been slowing down the adoption of 3D ICs based on TSV. The proposed monolithic 3D flow has the potential to overcome these barriers as it avoids the use of thick layers with lengthy etch and deposition processes. In fact, it can provide circuit fabrics for two strata at a cost that is less than one wafer substrate. Both the donor wafer and the carrier wafer are reusable. The porous layer processing could be done using batch processes and leverage technology developed by Canon [23] and enhanced for photovoltaic applications [20, 21]. As an indication for the cost of the porous/epi layer transfer process we can deduce from its current use for production of thin silicon for solar cell market. A US start up name Solexel just recently rose $31M [22] for such – *"Solexel is hoping to mass produce 35-micron-thick, high-performance, low-cost monocrystalline solar cells using a lift-off technology based on a reusable template and a porous silicon substrate."*

The bonding steps, both being non-precise, should cost less than $20. Accordingly, the porous substrates usage and the related additional steps cost should be less than the cost of a single wafer, making this proposed monolithic 3D flow very competitive cost-wise, while providing benefits beyond that obtainable with next node scaling.

Summary

Modified ELTRAN enables a simple path to monolithic 3D IC providing the best of all worlds:

- Vertical connectivity density comparable with horizontal density
- Use of existing transistor and interconnect flows
- Compatible with both advanced and older fabs
- Low cost and competitive with 2D IC cost structure
- Heterogonous integration: Fab lines, process nodes, device materials, processes
- Enables many new classes of devices and systems unattainable with 2D IC
- Multiple paths for cost reduction that were not possible with 2D IC
- Enabling efficient interconnect architectures

It seems that this new form of 3D IC offers a most attractive path to keep Moore's Law, while opening an unparalleled path for all fabs to keep enhancing their product range using their existing equipment and flows.

And yes, this opens a new horizon for the semiconductor industry.

Acknowledgement

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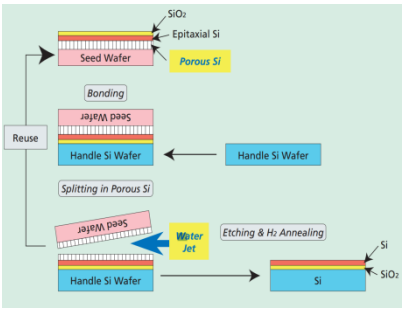

Fig. 1: ELTRAN (Epitaxial Layer Transfer) flow for SOI substrate fabrication

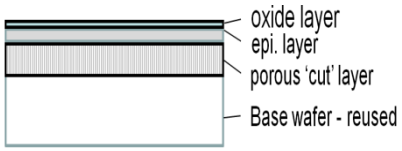

Fig. 2: Donor Wafer

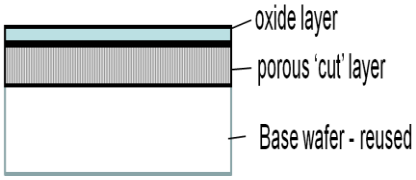

Fig. 3: Carrier Wafer

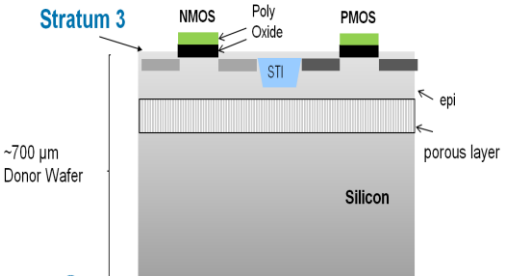

Fig. 4A: Donor wafer processed standard flow – Stratum-3

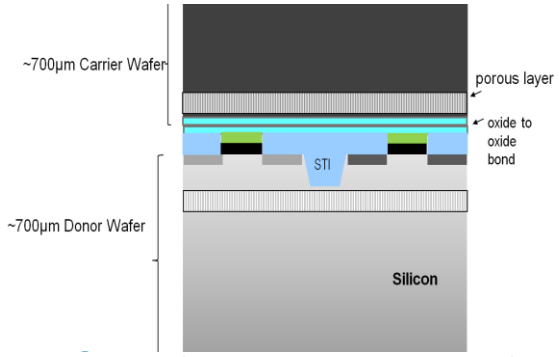

Fig. 4B: Stratum-3 flipped and bonded to a Carrier Wafer

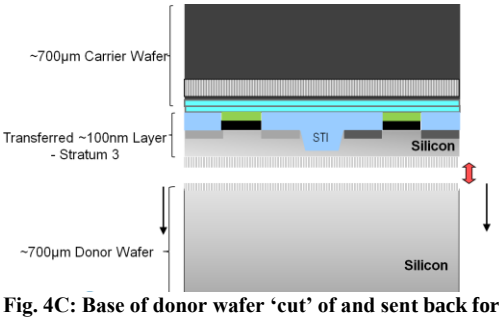

Fig. 4C: Base of donor wafer 'cut' of and sent back for reuse

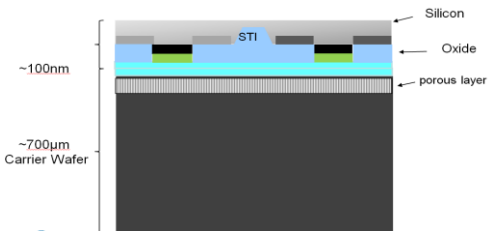

Fig. 4D: Porous residue cleaned and wafer 'flipped'

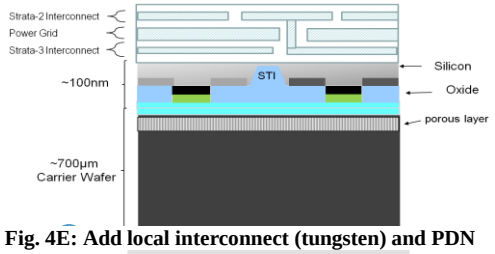

Fig. 4E: Add local interconnect (tungsten) and PDN

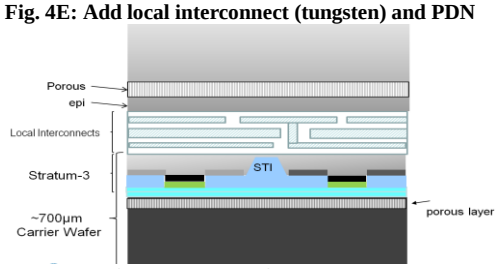

Fig. 4F: Perform layer transfer (ELTRAN or Ion-Cut)

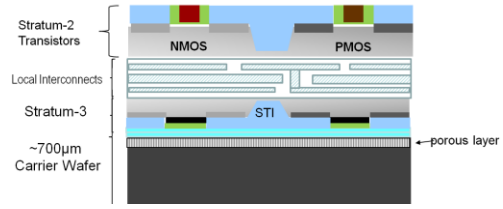

Fig. 4G: Cut, and process Stratum-2 aligned to Stratum-3

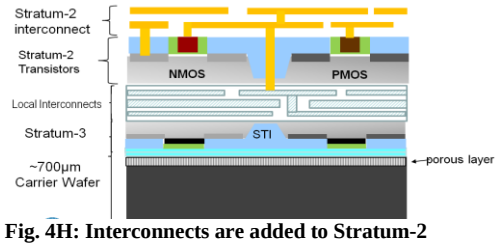

Fig. 4H: Interconnects are added to Stratum-2

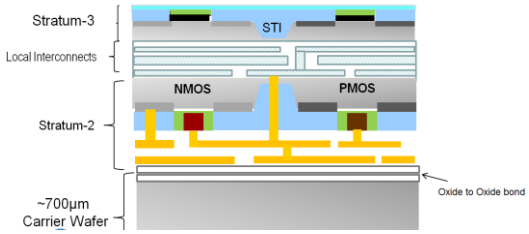

Fig. 4I: Flip, bond to Final Carrier, and cut carrier

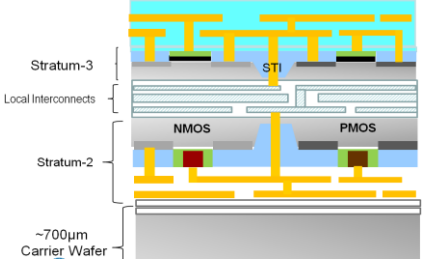

Fig. 4J: Interconnects are added to Stratum-3 => M3DI